SoC Prototyping Environment for Electromagnetic Immunity Measurements

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***Abstract*—We present a configurable standard environment for electromagnetic (EM) immunity measurement of prototype system-on-chip (SoC). The environment is composed of two boards compliant with the 62.132-2 and 62.132-4 IEC Std Parts, being conceived for radiated and conducted measurements, respectively. The SoC under test can be prototyped on two types of ICs: two FPGAs and a microcontroller. Practical experiments have been carried out. The obtained results demonstrate the utility and benefits from using the proposed platform to estimate in an early stage of the design process the behavior of embedded systems operating in EM environment.**

I. INTRODUCTION

The roadmap for standardization of immunity measurement methods has reached a high degree of success with the IEC 62.132 proposal [1]. Recently (2006), some extensions have been proposed through research publications, which aim at extending the *Bulk Current Injection Method* and the *Direct Power Injection Method* to 10 GHz [2].

At the same time, the technology scale down offers the possibility to design more complex integrated circuits (ICs) [3], with tenths of millions of transistors placed and routed in between more than one thousand I/O pins. The supply voltage is continuously decreasing, reaching less than 1 volt for the IC core, and less than 2 volts for the periphery and I/O pads. This scenario reduces noise margins and increases circuit susceptibility to external electromagnetic (EM) waves [4,5].

There has been an increased demand for EMC models applicable to integrated circuits and hardware/software-based prototyping vehicles, in order to conduct compatibility analysis early in the system-on-chip (SoC) design process. It is at this point that we introduce our work. We propose hereafter an innovative (configurable) platform for measuring the EM susceptibility of SoCs prototyped during the design phase. Depending on the designer interest and the target application, the prototype immunity can be measured with respect to the hardware and/or the software parts o the SoC. In the best of our knowledge, this is the first time that this kind of platform is reported.

The remainder of this paper is divided as follows: *Section 2* presents the proposed platform. *Section 3* describes the case-study and the practical experiment that have been carried out to demonstrate the utility and benefits from using the proposed platform. Finally, *Section 4* summarizes the main points of this work.

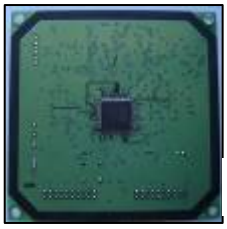
II. PROPOSED PLATFORM

The proposed environment is composed of two boards for radiated and conducted electromagnetic immunity measurements. With this infrastructure, multiple embedded microprocessors like MicroBlaze[1] and PowerPC 601 running uCLinux or uCOS-II[2] [6,7] can be prototyped. Additionally to the hardware parts, several implementations of VHDL-described embedded intellectual property (IP) cores and C-code programs can also have their immunity response measured and compared to each other in order to leverage the final dependability level for the SoC on the design.

Figure 1a presents a photograph of first board (Board I), designed and fabricated according the IEC 61.132-2 standard for radiated electromagnetic (EM) immunity measurement. The "*test side*" of this board is shown in Fig. 1a, which contains the IC under test (Xilinx FPGA, Spartan 300E). This side contains also the board ground layer. Fig. 1b shows "*other side*" of the board, which contains the remaining logic (SRAM memories, clock generator and voltage regulators, among other components). This board side also lays down the V_{DD} distribution network for the system. The two inner layers of the board are used for signal propagation. Around the board, it can also be observed a "*ground ring*" used to attach the onboard system ground with the TEM cell ground into a

[1] MicroBlaze™ is a true 32-bit soft RISC processor optimized for use in Xilinx's FPGA architectures. The processor's main memory interface conforms to the IBM CoreConnect specification for the On-Chip Peripheral Bus (OPB).

[2] MicroC/OS-II has been certified to RTCA DO-178B Level A for use in avionics systems where failure could result in catastrophic loss of the aircraft, and approved for use in FDA Class III medical devices where failure could result in loss of life for the patient or clinician.


(a)

(b)

Figure 1. Board I: 10x10cm2 IEC 62.132-2 std compliant board comprised by four-layers: Gnd (top) / signal / signal / Vdd (botton). (a) Top view; (b) Bottom view.

unique reference. Fig. 2 presents the basic blocks composing Board I.

The second board contains two Xilinx Spartan 500E FPGAs, a Texas 8051-like microcontroller, 16MBytes of SDRAM, and 8MBytes of serial Flash memory, among other glue logic required for communication with the test host computer (see Fig. 3 for details). In this figure, side (a) contains the components under test, i.e., the parts whose EM measurements can to be performed; whereas side (b) contains the remainder of the logic (processor bus, memories, crystals, connectors and external environment communication-support ICs, among other devices). Fig. 4 depicts the shielding box for radiated testing. The remainder logic of the board is protected inside the box, while the devices under test (FPGAs and microcontroller) are placed externally, to be exposed to EM fields. Fig. 5 presents the basic blocks of Board II.

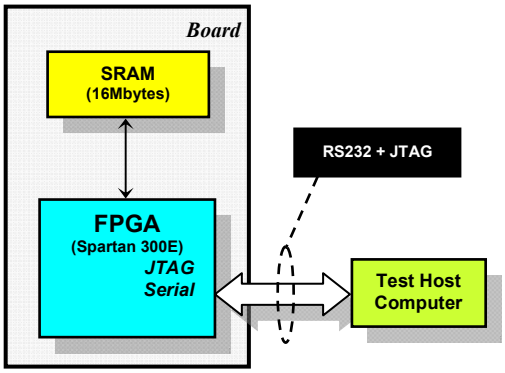


Figure 2. Basic blocks of Board I.

(a) (b)

Figure 3. Board II: IEC 62.132-4 std compliant board comprised of 6 layers for conducted immunity measurement. Views: (a) Top; (b) Bottom.

Figure 4. Shielding box for radiated test: (a) General view; (b) Inside the GTEM Cell.

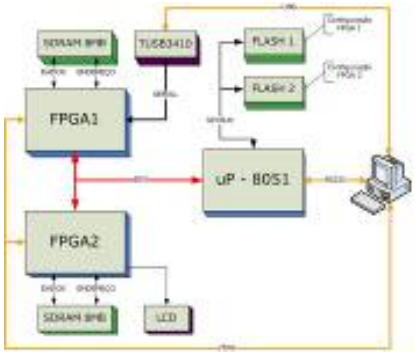


Figure 5. Basic blocks of Board I

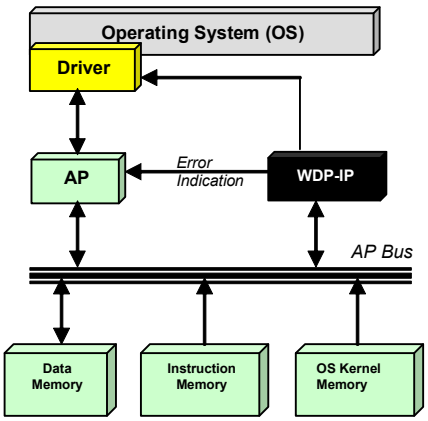
III. EXPERIMENTAL RESULTS

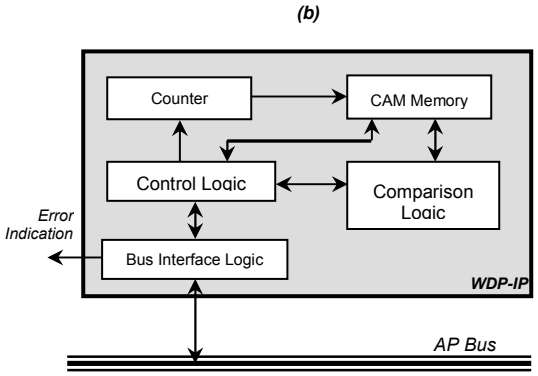
This section presents the *case-study* and the practical experiment that have been carried out to demonstrate the utility and benefits from using the proposed platform.

A. Case-Study

With this purpose in mind, we conducted an experiment aiming at analyzing the radiated electromagnetic sensitivity of a watch-dog processor intellectual property (WDP-IP) core [8,9] designed to monitor the Xilinx MicroBlaze soft core processor running under the uCOS-II operating system control. This system is said to be the "*Test Vehicle*", prototyped in Board I (Fig. 6a presents a general view of this system, whereas Fig. 6b depicts details of the WDP-IP core basic blocks). The whole SoC was described in VHDL language (VLSI Hardware Description Language).

(a)





(c)

Process ID	Idle	Counter	Bound Counter		Parity
			S_{lower}	S_{upper}	
0000	0	011…101	000…011	010…111	0
0001	1	000…101	000…111	010…001	1
…	…	…	…	…	…
n-1	0	000…101	000…011	111…000	1

Figure 6. SoC prototyped in Board I: (a) General architecture; (b) WDP-IP basic blocks; (c) CAM memory architecture.

Hereafter, it is presented a brief description of the WDP-IP basic blocks, as depicted in Fig. 6b:

1) Bus Interface Logic: This block is composed of two 16-bit registers, namely R-ONE and R-TWO. R-ONE is used by the processor to write a command to be executed by the WDP-IP (e.g., reset the whole CAM contents, reset only the Counter column of the CAM, perform a "ping" in the WDP-IP), whereas R-TWO is used to write a data to the WDP-IP or to read a data solicited by the processor from the WDP-IP.

2) *Control Logic:* The Control Logic is a very simple combinational circuit used to decode the commands received from the AP through R-ONE and to write/read data into/from R-TWO. This block is also responsible for managing the task scheduling process inside the WDP by loading/resetting the 32-bit counters of the Counter block and by interrupting the AP in the event of system error detection.

Another role of this block is to periodically reset the whole column "Idle" in the CAM Memory (Fig. 4). The periodicity by which this column is reset is defined by the maximum number of clock cycles that the processor is allowed to execute before returning control to run other slice of the same task again.

3) *Counter:* This block is a 32-bit counter with reset and preset commands used to count the number of clock cycles required by the processor to run a given task. The preset command is used to load the counter with the "Counter" field of the CAM Memory before continuing the count operation in the event of a context switching (task switch) controlled by the OS under the time-shared basis.

4) *Comparison Logic:* This block is basically a full-adder used by the Control Logic to determine whether the current counted number of clock cycles is in the clock cycles range [S_{lower} , S_{upper}] estimated for a given task.

5) *CAM Memory:* The memory fields shown in Fig. 6c are interpreted as follows: "**Process ID**" contains (4-bit) information about the name of the existing system tasks; "**Idle**" field (1 bit) indicates whether the time that a task is waiting for being executed by the processor is under a predetermined value; the (32-bit) "**Counter**" field shows the current number of clock cycles summed by the WDP-IP up to a given moment; the fields "S_{lower}" and "S_{upper}" (32 bits each) store the minimum and the maximum number of clock cycles computed system simulation for the processor to complete the execution of a given task; finally, the "**Parity**" field contains the parity bit for the whole line of the CAM memory. This bit is used by the WDP-IP to run a sanity check, when requested by the processor.

Aiming at accessing the WDP-IP, a dedicated *driver* was written in C-ansi, and compiled with the OS kernel. By means of this driver, the processor informs the WDP-IP about the beginning and completion of user tasks. On the other direction, the WDP-IP uses this driver to signal to the processor a system failure or to periodically indicate its own health status.

The driver contains two functions. The first one is "*ip_cmd*", which is used by the Xilinx MicroBlaze to write instructions into R-ONE and write data into R-TWO to the WDP-IP, or read data stored in R-TWO by the WDP-IP. The second function is "*ip_sw*". This is used by the processor to indicate to the WDP-IP to switch from one task to another. When this command is used by the Xilinx MicroBlaze, the WDP-IP understands that it must switch from one task to another (by saving the context of the first task in its CAM Memory and by recovering the context of the second one also from this memory).

Figure 7 depicts the basic communication sequence between processor and WDP-IP during a multi-task execution. When the Xilinx MicroBlaze starts running a task, it signals to the WDP-IP (Fig. 7: command "*ip_cmd*") to reset the counter and then, start counting from "zero" the number of clock cycles needed by the processor to execute such a task (in Fig. 7, this command is used once at the first time tasks #1, #2 and #3 are executed). When the OS switches context, moving from one task to another, the Xilinx MicroBlaze signals to the WDP-IP (Fig. 7: "*ip_sw*") to perform the following actions: *(a)* save the current counter value for the leaving task (the one going to background) into the CAM Memory; *(b)* reload the counter with the partial value stored in the CAM Memory for the next task in the OS waiting list (the one coming to foreground) and increment the counter from this value on, till the moment when the task is switched back again to the "*wait*" state (background). This process is repeated as many times as the task is run, until its complete retirement by the processor.

Note that the communication process between the processor and the WDP-IP is done by the OS under the "*supervisor*" mode control. In addition to allow application programs to be compiled "as they are", i.e. with no modifications, this condition also increases system reliability

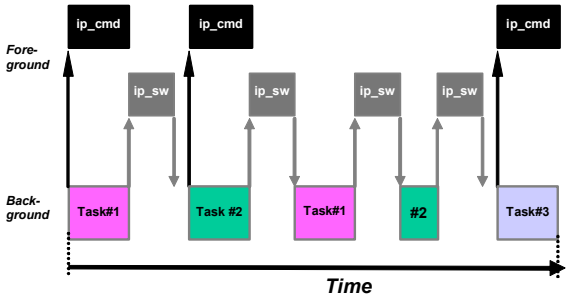


Figure 7. Basic commands and communication sequence between the Xilinx MicroBlaze and the WDP-IP during normal system operation.

since any communication with the WDP-IP has the priority and the security native from the OS instead of the application programs ones.

B. *Practical Experiment*

To perform the experiment, we implemented three user tasks running in the processor under the time-shared basis: a random prime numbers generator (PNG), a bubble sort to reorder a matrix (BS), and a digital filter (DT). This experiment was based on the International IEC 62.132 Standard Part 2: Measurement of Radiated Immunity – TEM Cell Method.

Figure 8 depicts the TEM-Cell and the test setup at the Instituto Nacional de Tecnologia Industrial – INTI, Buenos Aires, where the experiment was conducted. Dealing with minimizing test procedure complexity, we arbitrarily decided to stop the experiment when we succeeded to obtain 330 measurements of system failure. This resulted in a total time of system exposition to radiated EMI of approximated 40 hours. The test conditions were as follows:

a) EM field range: from 10 to 220V/m;

b) Measured frequency range: from 150KHz to 3GHz (extended IEC 62.132-2);

c) Signal Modulation Format: three different types were used: 80%, Without Modulation, and Pulsed Signal.

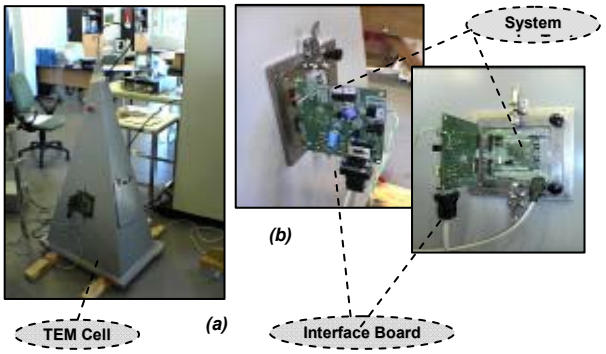


Figure 8. Test environment showing TEM Cell and test vehicle prototyped in Board I. (a) General view; (b) and (c) Closer views detailing the test vehicle with the FPGA board side turned into the chamber.

The Interface Board observed in Fig. 8b and 8c is used to perform communication between the Test Vehicle and the external computer (test host). The Interface Board is responsible, for instance, for the RS232 serial and for the JTAG communications between the test engineer and the Test Vehicle during measurements procedure.

It is worth noting that we have also implemented a second version of the WDP-IP. This version presented the same functionalities as the WDT-IP in hardware, but it was implemented purely in software (C-ansi) and compiled with the kernel of the uCOS-II OS.

Additionally, the fault detection capability of the proposed I-IP was compared against the uCOS-II OS native fault detection structures existing in its own kernel. In summary, test measurements were carried out on three different system configurations: (a) microprocessor + WDP-IP in hardware (VHDL); (b) microprocessor + WDP-IP in software (C); and (c) microprocessor + uCOS-II OS native fault detection structures (original uCOS-II OS kernel). Fig. 9 summarizes the measurements for this experiment.

Figure 10 presents the occurrence of faults as a function of the: modulated EM signal frequency (Fig. 10a) and the EM field incident on the board under test (Fig. 10b). For instance, in the frequency range of 100-200MHz (Fig. 10a), the system under test presented 265 faults: 174 (65.7%) were detected by the WDP-IP in hardware, 88 (33.2%) were detected by the WDP-IP in software, and 3 (1.1%) were detected by the native fault detection structures existing in the kernel of the uCOS-II OS.

Table 1 summarizes the main characteristics of the WDP in hardware. The area overhead is computed with respect to the one required to lay down the MicroBlaze processor.

TABLE I. OVERHEADS MEASURED FOR THE WDP I-IP.

Area	Memory (Bytes)	Performance Degradation (ms)
11.90% (Configurable Logic Blocks)	0.77% (OS-Kernel Driver for the WDP)	Negligible (some assembly-level macros are inserted in the OS kernel to perform CPU-WDP communication)

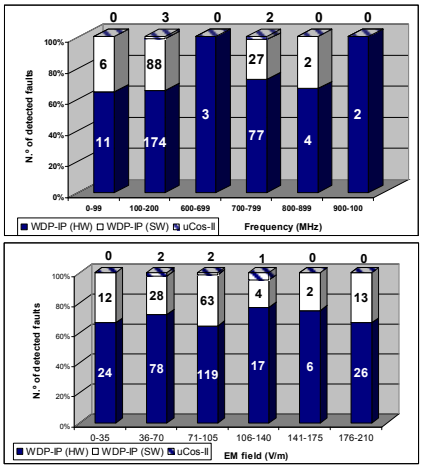


Figure 9. Fault detection capability measured for the I-IP approach during IEC 62.132-2 test session: Approaches comparison and Classification of observed errors.

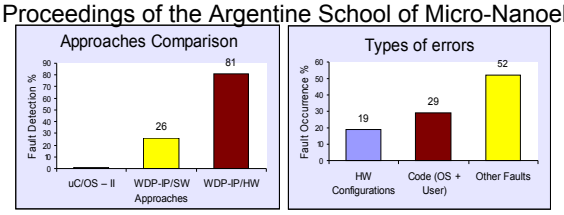


Figure 10. Fault occurrence as a function of the modulated EM signal frequency (a) and the EM field incident on the board under test (b).

After analyzing the measurement results, we concluded that:

- The uCOS-II kernel native fault detection was very low (approx. 1%) because of the embedded structures were able to detect only those faults that resulted in an increase of the time allocated by the OS for the processor to run the task slices. Note that those faults that reduce the time allocated by the OS (for instance, resulting in a procedure aborting) are not detected by the kernel native structures.
- The WDP-IP software version was capable to detect (in addition to those faults that resulted in an increase/decrease of the time allocated by the OS for the processor to run the task slices) most of the faults that affected user memory elements (FFs and SRAM). However, it failed to signal most of those faults that changed the FPGA configuration bitstream. Several of these faults yielded system crash (processor should be reinitialized).
- The WDP-IP hardware version was capable to detect most of the faults that affected not only user memory elements, but also those that corrupted FPGA configuration logic. In addition to this, the WDP-IP also detected those faults that corrupted (by increasing or reducing) the task slice execution time frames defined by the OS.

IV. CONCLUSIONS

There has been an increased demand for hardware/software-based prototyping vehicles in order to conduct compatibility analysis early in the system-on-chip (SoC) design process. In order to address this point, we presented a configurable standard environment for electromagnetic (EM) immunity measurement of prototype system-on-chip (SoC). In the best of our knowledge, this is the first time that this kind of platform is reported.

The environment is composed of two boards compliant with the 62.132-2 and 62.132-4 IEC Std Parts, being conceived for radiated and conducted measurements, respectively. The SoC under test can be prototyped on two types of ICs: two FPGAs and a microcontroller.

The underlying advantages of the proposed test platform rely on: (a) reduction of SoC design cost and time due to early-estimation of system behavior in the presence of EM noise according to recognized standards, and (b) allowance of measurements for hardware (IP cores) as well as for software (user-code and operating system-kernel).

Practical experiments have been carried out. The obtained results demonstrate the utility and benefits from using the proposed platform to estimate the behavior of embedded systems operating in EM environment.

ACKNOWLEDGMENT

The work reported in this paper has been partially funded by CNPq (Science and Technology Foundation, Brazil).

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