Wide Range Neutron Flux Measuring Channel for Aerospace Application

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Abstract. The use of classical techniques for neutron flux measurements in nuclear reactors involves the switching between several detection chains as the power grows up to 10 decades. In space applications where mass and size constraints are of key significance, such volume of hardware represents a clear disadvantage. Instead of requiring different instruments for each reactor operating range (start-up, ramping-up, and nominal power), a single instrument chain should be desirable. A Wide Range Neutron Detector (WRND) system, combining a classic pulse Counting Channel with a Campbell's theorem based Fluctuation Channel can be implemented for the monitoring and control of a space nuclear reactor. Such an instrument will allow for a reduction in the complexity of space-based nuclear instrumentation and control systems. In this presentation we will discuss the criteria and tradeoffs involved in the development of such a system. We will focus particularly on the characteristics of the System On Chip (SOC) and the DSP board used to implement this instrument.

Keywords: Space reactor instrumentation, wide range neutron flux measurements, signal processing electronics.
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INTRODUCTION

Although there is still too much information to be gathered about our solar system neighborhoods (Moon, Mars, Venus, Mercury), the farther planets are the ones that attract the most of our attention. In this field, the use of nuclear power for energy or even propulsion is beginning to be considered as the best alternative (Bennett, 2006). All the systems involved in space missions have to be not only highly reliable as usual in nuclear fields but also light in weight, small size and low power. In this sense, the classical technique to measure the power generated in the core of nuclear reactors, involving the switching between several detection chains as the power grows along up to 10 decades of neutron flux results inapplicable.

The combined use of pulse and fluctuation modes of a fission chamber is becoming a common practice for Wide Range Neutron Detection in terrestrial applications (Kropik, 2000). A Wide Range Neutron Detector (WRND) has been already developed, tested and installed at the OPAL (Open Pool Advanced Light – Water Reactor) in Australia (Gonella, 2004), being now full operative (see figs. 1a and 1b). However, the analog signal processing section of this system presents several drawbacks in relation with its use in space due to signal drifts and components aging under radiation effects, especially when it is intended for long term missions. Digital systems equivalent to that are cited in the literature (Lescop, 2000), but just intended for terrestrial use. We present here the DSP electronics of a digital WRND, specifically designed to be used in neutron flux measurement for control and protection systems of a nuclear reactor in space missions.

SYSTEM

The WRND (Dc – 045 model) wide range "Campbellian" system is basically a fission detector (Nassif, E. et al, 2007) with adequate electronics, able to operate in pulse mode at low neutron flux and in current fluctuation mode at medium and high neutron fluxes. The electronic side of this system has been implemented using a triple redundant
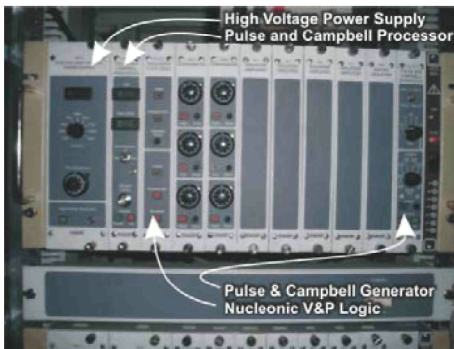
(a) Electronic Modules.   **(b)** Fission Chamber.

FIGURE 1. WRND System Currently Being Installed at the Australian Research Reactor.

VME bus (see Figure 2) over which three identical units are mounted. Each unit is composed by an analog signal conditioning board, a Digital Signal Processor (DSP) board, a Single Board Computer (SBC), an I/O board and a 1553 Standard Communication board. The full system is composed by these three modules, a triple redundant power conditioning module, a Final Actuation Logic board and the fission detector.

Analog Board

This board contains a High Voltage Power Supply, a pulse shaping amplifier for the pulse region of the detector output and a wide band amplifier for the fluctuation region. Considering the low level of the signals involved in this board, a very careful grounding and shielding of all its areas is required. The design requires special attention to the input circuits and to the cable used to carry the signal from the detector output.
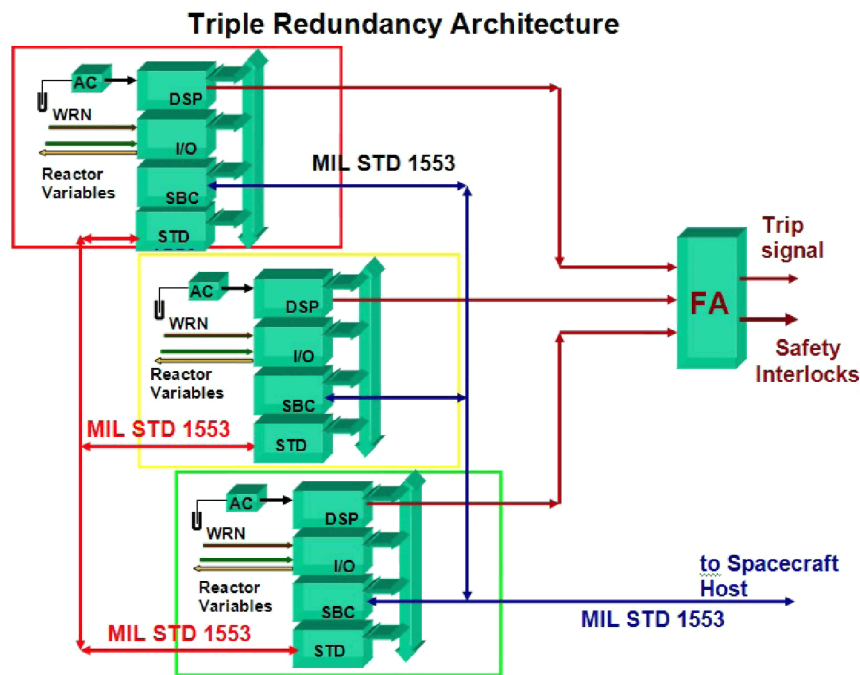

FIGURE 2. Block Diagram of the WRND System.

CPU Board

This board is a high performance, low power and fault tolerance single board computer for space applications based on SPARC chip ATMEL TSC-695F. The board is capable of standard VME interfacing with master features.

DSP Board - Functional Description

The WRND operates taking advantage of two of the three modes of operation of the fission chamber. This chamber produces pulses with a count rate proportional to the neutron flux, in the lowest zone of the neutron flux measurement range. Above this zone, the pulses begin to "pile up" and a random fluctuation type of signal comes out of the fission chamber. This is called the fluctuation operation mode of this detector also called Campbell mode.

Campbell (Campbell and Francis, 1946; DuBridge, 1967; Thomas and McBride, 1968; Knoll, 1992) demonstrated that there is a relation between the estimated statistical moments of this signal and the neutron flux. It is possible to obtain an estimation of the neutron flux using the first statistical moment (mean) but with high background gamma noise (Matatagui and Sabaté Puignal, 1980). As the order of the moment is increased the influence of this noise decrease, but the statistical uncertainty get also increased. A good trade off (Baers et al, 1993) is the use of the second statistical moment (conventional variance).

With this DSP board, it is possible to obtain an accurate estimation up to the sixth decade of neutron flux using the pulse mode. Also, the variance of the signal becomes a reasonable measure of the flux above the fourth decade. This allows an almost two decade transition zone where a convenient switching of the data stream can be produced by automatic means.

Board Implementation

The WRND Digital Signal Processing Module is being implemented on a 6U format VME board using engineering versions of space qualified components. This board receives both, the amplified shaped Gaussian pulses related with the lowest decades of the reactor neutron flux and the fluctuation signal produced by the fission detector operating on its Campbellian region of operation. The block diagram of the board can be seen in Figure 3.
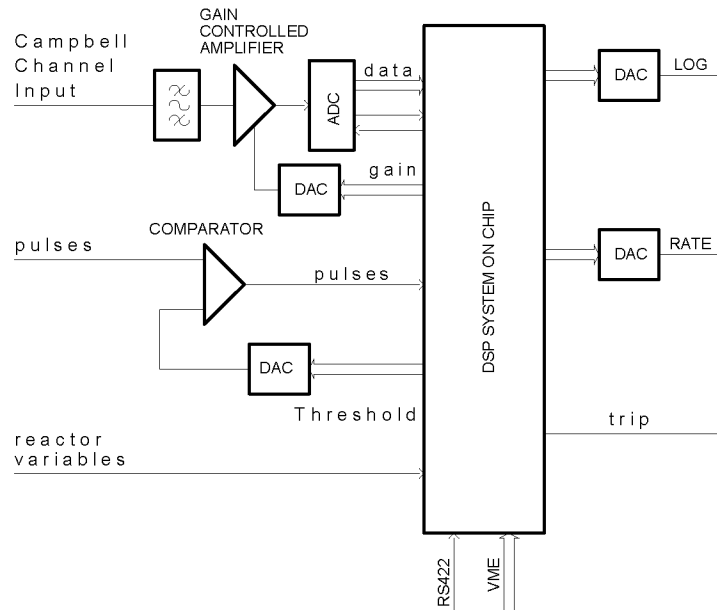

FIGURE 3. Block Diagram of the DSP Board.

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The fluctuation signal is filtered using a passive bandpass filter in order to suppress the cero and aliasing frequencies components and then transfer them to the A/D converter through a variable gain amplifier. This gain can be set digitally from a host computer to compensate from the calibration degradation of the system by the aging of the detector and the analog electronic components. The nuclear shaped Gaussian pulses are discriminated by energy and counted. The discriminator threshold can be digitally set from the host computer.

All the configuration parameters of the board can be modified from the SBC board by VME bus accesses. A serial RS422 communication channel is also provided. The signal processing on the board is carried out by a DSP System On Chip. The DSP SOC produces a digital reading of the reactor core neutron flux in logarithmic scale along with the rate of this flux for control purposes and a trip request signal for safety actions. Full range output from pulses and Campbellian channels can also be achieved.

Although the DSP SOC has been prototyped over two reprogrammable FPGA devices, its code has been written using a transportable – technology independent – style, opening the door for single chip implementation and making it possible the migration towards radiation tolerant devices with minimum engineering rework.

DSP SOC DESCRIPTION

The DSP SOC operation can be described by the flow diagram shown in fig 4. This operation is achieved through the contribution of two different operative areas: the Communication Section and the Processing Section in the following way:
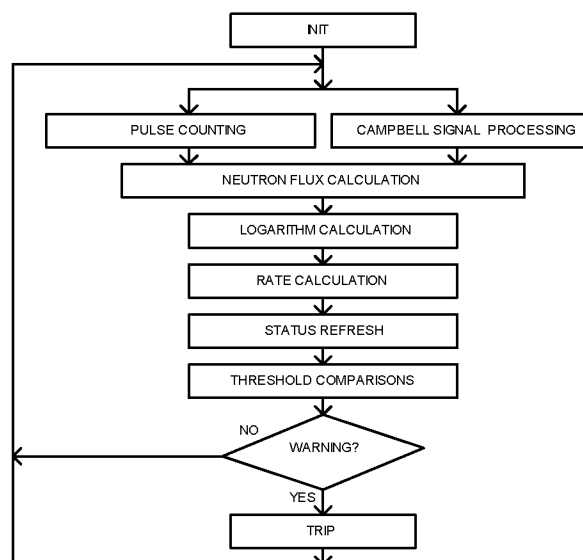

FIGURE 4. Flow Diagram of the DSP Board Operation.

The Communication Section is involved on the functions of changing or monitoring configuration parameters and transfer log scale neutron flux and rate data from the Processing Section through the WB/WB Bridge to the serial RS422 port or VME bus driver. These functions are achieved through the use of specific commands originated on an external processing device. It also feeds two D/A converters to provide an analogue version of the log scale neutron flux and rate data stream outputs.

The Processing Section is the responsible for polling the Pulses and Campbell front end modules, processing the raw data coming from them and finally evaluate if the flow and rate values determines the conditions needed to make a trip requirement.
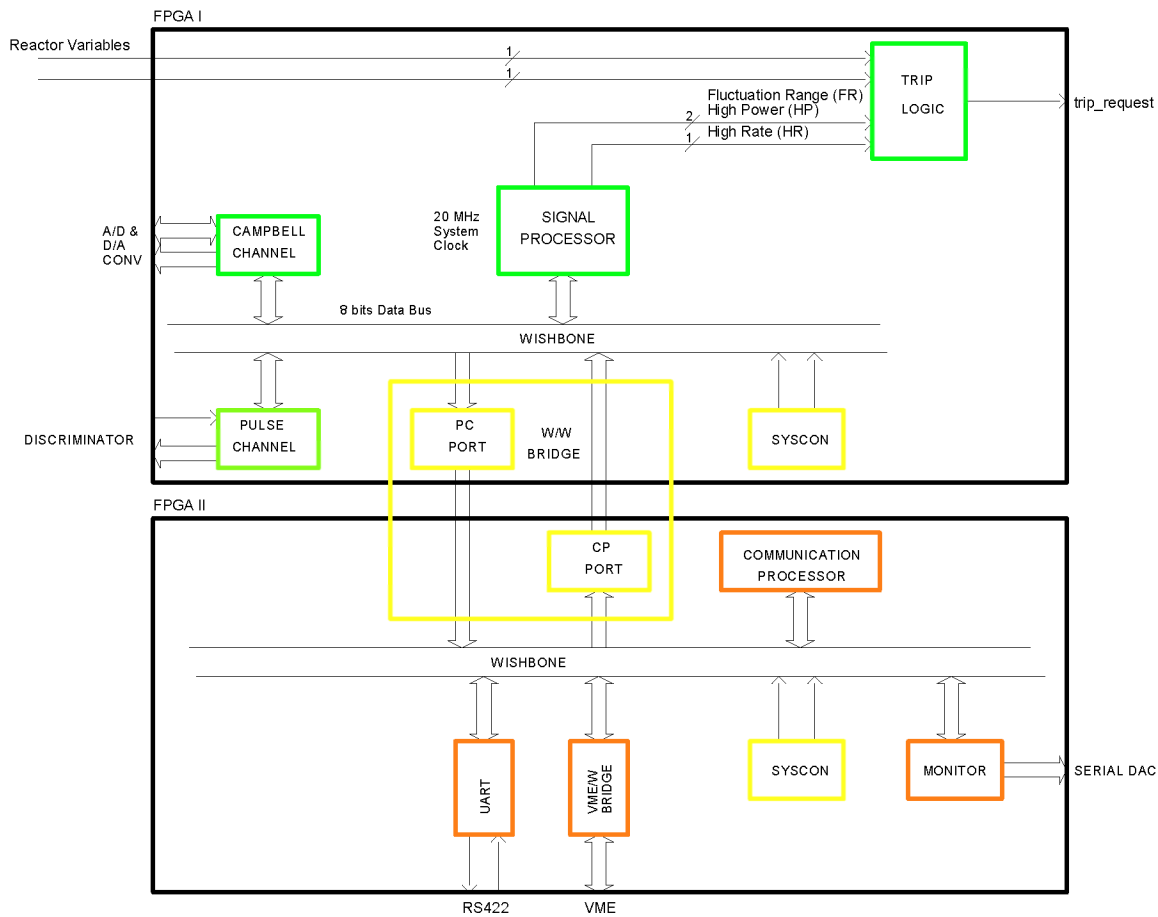
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FIGURE 5. Block Diagram of the DSP SOC.

Figure 5 shows the internal structure of the DSP SOC. Apart from the functional division in two sections, the SOC has been distributed physically between two different devices in order to allow its implementation on low density FPGAs with space heritage.

The internal logic of these sections is implemented using a standard bus (WISHBONE) over which RTL level blocks (cores), written in VHDL language are integrated.

The need to use more than one FPGA to implement the processing logic, calls for special precautions in the design of the general clock network of the entire system.

Another consequence of the distribution of the logic in more than one device, is the need to use independent buses and with that, independent systems on each one of them. In order to allow communication between both systems the buses have to be interconnected by means of a WISHBONE/WISHBONE bridge.

We have chosen an implementation of the WISHBONE bus (Opencores) with the following characteristics: shared type, 8 bits data bus and 8 bits address bus. The operating frequency of the bus clock will be 20 MHz.

Processing Section - Signal Processor

The processor reads the outputs of the Front End Pulse Channel Module and the Front End Campbell Channel Module. After that, both are scaled. Although their contributions are produced over different parts of the neutron flux range, there is an overlapping region between them. In order to prevent non-linear behavior in the system operation, the way in which both channels contribute to the flux value calculation is controlled by the algorithm showed in Figure 6.
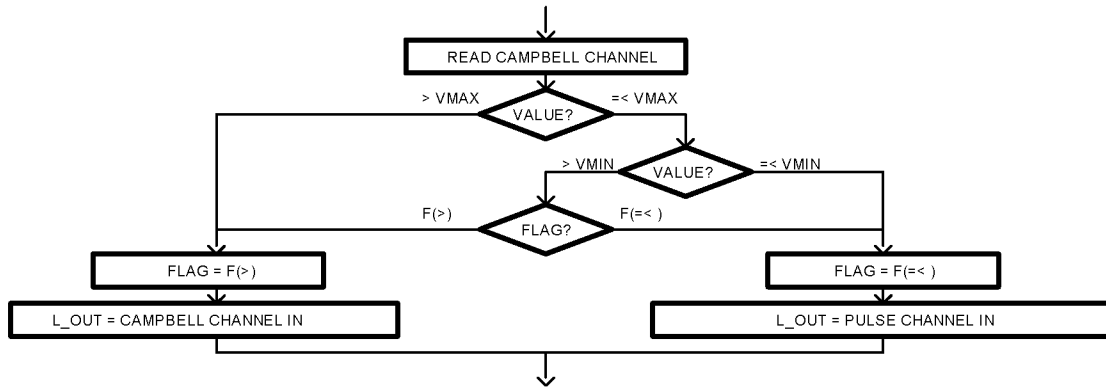

FIGURE 6. Flow Diagram of the Data Stream Switching.

As it can be seen here, the Campbell Channel data is always taken as a reference. If its value is greater than VMAX (which is always in the upper part of the overlapping region) the only contribution to the calculation of the flux will be the Campbell channel.

If the Campbell Channel data has a value below VMIN, the only contribution to the calculation of the flux will be the Pulse channel. In the case where the Campbell Channel data has values between VMAX and VMIN, the contribution of both channels will depend on the sign of the variation of the flux.

The decimal logarithm of this data stream is calculated. The output data word will be 32 bits floating point. It becomes necessary to insert a low-pass filter between the logarithm calculation stage output and the rate calculation stage input, because of the noisy nature of the signal. The rate calculation block is also implemented as a digital filter.

Pulse Channel Front End

This module counts the amount of rectangular pulses that comes from the pulse channel discriminator during a time interval called integration period. The module has two operation modes: the one period and the multi-period mode. The first one consists on a simple integration procedure that store its results directly on the Pulse Channel Front End output register. The second mode accumulates the partial outputs of a sequence of multiple integrations until a suitable result is achieved.

The switch between both modes is determined by a control algorithm that minimizes the value of the statistical uncertainty in the final result.

This module begins its integration every time the signal processor executes a polling operation over it. The integration finishes 1/256 seconds after that.

Campbell Channel Front End

This block calculates the square average of 1024 samples from the filtered fluctuation signal. This module begins its integration every time the signal processor polls it and finish at less than 1/256 seconds after that. Once finished the calculation it store its result in an output register and wait for the next signal processor polling.

Trip Logic

The processing section use the calculated results in combination with external processes status signals to determine predefined trip conditions. This produces a digital Boolean output that calls for trip when are fulfilled that conditions.

Communication Section

The communication Section checks periodically the Rx channel from the UART and internal registers from the VME/WB Bridge, in order to verify the arrival of external commands and transfers neutron flux and rate data from the WB/WB Bridge PC Port, toward the analogue output ports (D/A converters).

Communication Processor

The Communication Processor acts as a communication master for the commands that come from the serial data port and the VME/WB Bridge. Except for the periodical refresh of the analogue outputs and inspection of the UART Status Register and internal registers of the WB/WB Bridge, all the other functions of this master are conditioned to the commands coming from the local SBC or remote host computer.
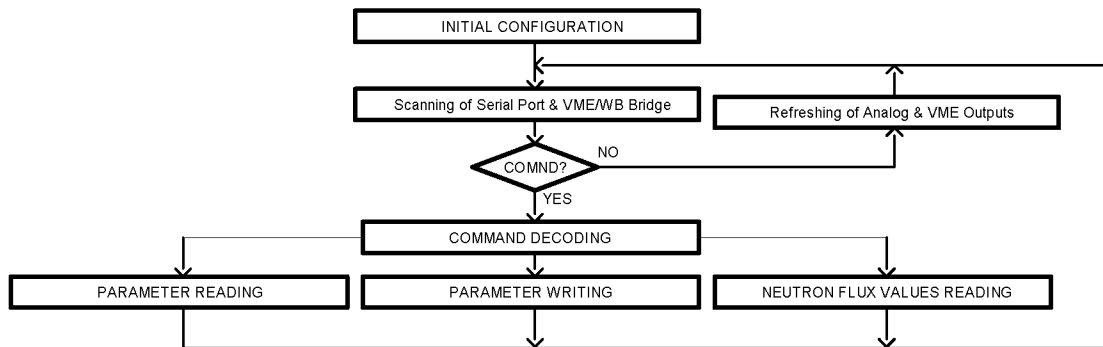

FIGURE 7. Flow Diagram of the Communication Processor Operation.

Three different types of functions can be serviced by this processor: the change of configuration parameters, the reading of current parameters and the reading of neutron flux related data (see fig. 7).

UART

As in the case of the interface with the VME bus, the UART block is used to configure the board or monitor the processing results and the status of the logic. As the aim is to achieve a significant economy of the silicon area occupied in the FPGA, this block will be customized to operate with a fix communication configuration in parameters such as speed, parity, and word format.

VME/WB Bridge

The DSP board registers may be accessed from an external intelligence through the VME bus. This access is made possible by a VME/WISHBONE bridge that withstands up to 16-bit-wide data words. This block may be used to configure the board or monitor the results of the processing and the status of the logic.

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A digital driver for two analog outputs corresponding to LOG and RATE signals will be provided, just for debugging purposes.

The Processing and the Communication sections interact through the WB/WB Bridge Ports. This bridge has two ports.: CP Port and PC Port. Both of them are unidirectional. The CP Port allows the writing of configuration parameters from the Communication Section to the Processing Section while PC Port allows the reading of the Configuration Parameters and the transference of log scale neutron flux and rate data towards the processing section.

Each port is basically a dual port RAM memory that can be written from one section and read from the other. The use of internal control logic in the RAM WISHBONE interfaces on input and output, and the microcontrollers wait state capability prevents the occurrence of metastability effects in the data transference between both sections.

RESULTS AND DESIGN TRADE OFFS

A prototype version of the DSP board was tested under real conditions in the RA6 reactor. This facility is a 500kW thermal power reactor for research and training that was built by INVAP (1982) and operates on the premises of the Centro Atómico Bariloche belonging to the Argentine Nuclear Authority, the CNEA. It is an open-pool reactor, designed to use 20% enriched Uranium fuel, and is moderated and cooled by light water. Figure 8 shows the measured power (from the processed outputs of the Pulse and Campbell Channels) versus the real reactor power (inferred from the reference current of the reactor control system). From the graph can be seen that the board allows the measure of the reactor power along all its range (0 to 5×10^5 watts) with a maximum full scale error less than 1%. The switching between channels in the suitable point allows to keep low the value of the power calculation error by discarding the low accuracy data zones. The neutron flux measurements (not seen in the figure) showed a Campbell Channel operative range from 10^4 to 10^{10} nv and a Pulse Channel operative range from 10^0 to 10^6 nv.
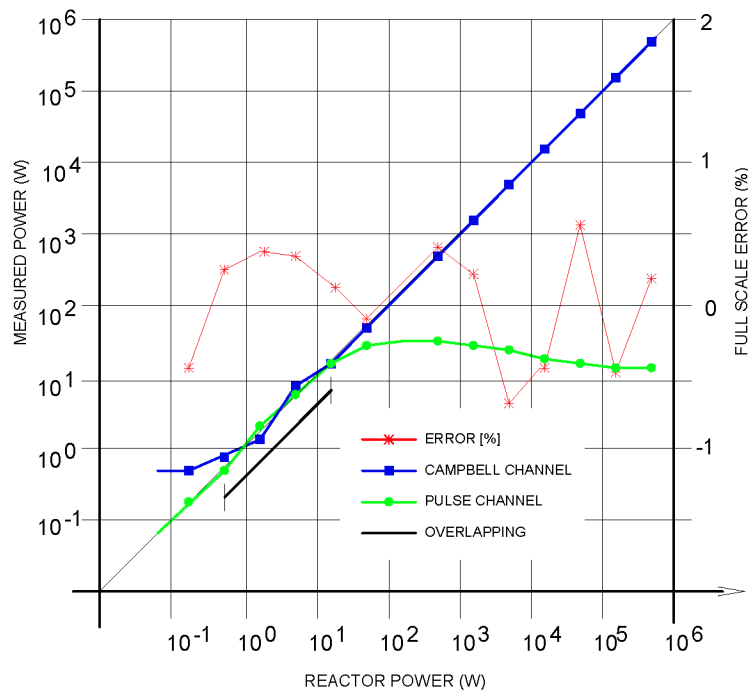

FIGURE 8. Experimental Results in RA6 Reactor.

The upper limit of the Pulse Channel comes from the pile up of the pulses while the lower limit of the Campbell Channel comes from gamma activity background and thermal noise on electronic devices. The influence of gamma activity background could be diminished by the use of higher orders of Campbell and the influence of noise could be

reduced by the use of cross correlation of the Campbell signal. However, both improvements from the point of view of the extension of the overlapping region, requires a more complex electronics and with this an increase in the number of failure modes of all the system. An almost two decades width overlapping region is good enough to allow a smooth transition between the two neutron flux measurement processes (pulse count rate and fluctuation signal variance). To prevent from erratic switching between both channels because of the statistical uncertainty of the measurement, a hysteresis behavior is provided around the switching point.

The switching decision depends on the value of the Campbell Channel output. The use of the Pulse Channel output value, although better from the point of view of the statistical uncertainty of the measurement, results unreliable. This is because at high neutron flux, its behavior becomes ambiguous and repeats the characteristic values of lower flux but with decreasing tendency.

Also, as the WRND output has to reflect the flux changes with minimum delays but without increasing too much the statistical uncertainty, a sampling period of 5 ms was chosen. In the case of the Pulse Channel a measurement period of that length produces an unacceptable fluctuation of the output for low count rates. In order to overcome this problem, a control mechanism has been provided to change the length of the counting period from 4 ms to 1 s in steps of 4 ms to keep the statistical uncertainty at a minimum.

SPACE ENVIRONMENT TOLERANT DESIGN

Although, in this phase of the development the board has been implemented using COTS parts, all of them have been carefully selected to have equivalent versions that fulfill radiation tolerance, high reliability and extended-range temperature characteristics. The board has been ruggedized in order to resist the impact of any stress coming from spacecraft acceleration. Any possible failure of the system has been mitigated at system level by using (see fig. 2) triple redundancy. Reliability has been enhanced by significantly reducing the number of electronics parts on the board. Most of the functions on the board are digital and all digital mechanisms are included inside two rad tolerant antifuse technology FPGAs (see fig. 5). SEU and SEFI radiation effects are mitigated by using hard-wired TMR flip-flops for internal registers. The software for the communication and processing sections runs directly from internal ROMs and both processors uses Watch Dog Timers to fulfill availability requirements.

CONCLUSIONS

A Wide Range Neutron Detector system has been upgraded, according to specifications on WRND NASA SBIR Phase II Report (Merk, 2005), with the digital processing of its signals. The digitalization of these processes allowed a high integration of this part of the electronics, increasing in this way its reliability. Although the DSP board is at the prototype stage of its development, several design considerations has been done in order to produce a design that will allow the flight model to fulfill space mission requirements, such as component selection and technology independent code design.

NOMENCLATURE

ADC = Analog to Digital Converter
CNEA = Comisión Nacional de Energía Atómica
COTS = Commercial off the shelf
DAC = Digital to Analog Converter
DSP = Digital Signal Processor
FPGA = Field Programmable Gate Array
IEEE = Institute of Electronic and Electrical Engineers
INTI = Instituto Nacional de Tecnología Industrial
LOG = Logarithmic scale neutron flux
MHz = Megahertz
OPAL = Open Pool Advanced Light-Water Reactor
RAM = Random Access Memory

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RATE = Rate value of the LOG signal
RTL = Register Transfer Level
SBC = Single Board Computer
SEFI = Single Event Functional Interrupt
SEU = Single Event Upset
SOC = System On Chip
UF = Uncertainty Factor
UART = Universal Asynchronous Receiver Transmitter
VHDL = VHSIC Hardware Description Language
VHSIC = Very High Speed Integrated Circuit
VME = Versa Module Eurocard
WB = Wishbone bus
WRND = Wide Range Neutron Detector

ACKNOWLEDGMENTS

REFERENCES

Baers L.B., et al., "Use of Higher Order Signal Moments and High Speed Digital Sampling Technique for Neutron Flux Meassurement," *IEEE Trans. Nucl. Sci.*, **VOL. 40**, NO. 4, August 1993.

Bennett G. L.,"Space Nuclear Power: Opening the Final Frontier", AIAA-2006-4191, *presented at the 4th IECEC*, Published by AIAA, June 2006.

Campbell, N.R. and Francis,V.J., "A Theory of Valve and Circuit Noise," *Journal of IEEE*, **Part III** 93 (1946).

DuBridge, R.A., "Campbell Theorem – System Concepts and Results," *IEEE Trans. Nucl. Sci.*, **NS 14**, No **(1)**, 241 (1967).

Gonella, J.L., *"Informe de Ensayo canal Campbell serie cero,"* GPES-6124-3AEEL-002-A, INVAP (Applied Research Company), Bariloche, Argentina, 2004.

Knoll, G.F., *Radiation Detection and Measurement*, John Wiley & Sons, NY, NY, 1992, pp. 534-538.

Kropik, M., "Neutron Flux Measurement utilizing Campbell Technique," *Proceedings of the International Conference Nuclear Energy in Central Europe 2000*, , editor/publisher Hanser, Munchen, ALLEMAGNE (1987) (Revue), Bled, Slovenia, September 11-14, 2000.

Lescop, B. et al, "Marine: a fast fully digitalized wide range neutron monitor system," *Nuclear Science Symposium Conference Record, 2000 IEEE Volume 1*, Issue , 2000 Page(s):5/86 - 5/90 vol.1, editor/publisher IEEE Society.

Matatagui, E. and Sabaté Puignal, P., "Técnica de Fluctuaciones para medición de Flujo Neutrónico," in *Proceedings of IX ReuniónCientífica AATN (Nuclear Technology Argentine Association)*, edited by AATN (Asociación Argentina de Tecnología Nuclear), Buenos Aires, Argentina, 1980.

Merk,J., *Wide Range Neutron Detector Phase II Report*, Proposal # X2.02-7802, NASA SBIR Contract No. NNC06A15C, Payload Inc., Boston, MA, 2005.

Nassif, E. et al., "A Wide Range Neutron Detector for Space Nuclear Reactor Applications." *In the proceedings of Space Technology and Applications International Forum (STAIF 2007)*, edited by M.S. El-Genk, AIP Conference Proceedings No., Melville, New York, 2007, pp. 185-194.

Opencores, *"Specification for the WISHBONE System on Chip (SoC) Interconnection Architecture for Portable IP Cores,"* http://www.opencores.org/projects.cgi/web/wishbone/wishbone, accesed July 20, 2003.

Thomas, H.A., and McBride, A.C., "Gamma Discrimination and Sensitivies of Averaging and Rms Type Detector Circuits for Campbelling Channels," *IEEE Trans. Nucl. Sci.*, **NS 15**, (1), 15 (1968).