1454 IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 62, NO. 6, JUNE 2013

Graphene Epitaxial Growth on SiC(0001) for Resistance Standards

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***Abstract*—A well-controlled technique for high-temperature epitaxial growth on 6H-SiC(0001) substrates is shown to allow the development of monolayer graphene that exhibits promise for precise metrological applications. Face-to-face and face-to-graphite annealing in a graphite-lined furnace at 1200 °C–2000 °C with a 101-kPa Ar background gas lowers the rates of SiC decomposition and Si sublimation/diffusion and thus provides a means to control the rate of graphene layer development. We studied a wide range of growth temperatures and times and describe the resulting sample surface morphology changes and graphene layer structures. The experimental results are compared to a kinetic model based on two diffusion processes: Si vapor diffusion in the Ar-filled gap and atomic diffusion through graphitic surface layers.**

***Index Terms*—Diffusion processes, epitaxial growth, graphene, quantized Hall resistance (QHR) standard, quantum Hall effect, surface morphology.**

I. Introduction

GRAPHENE is a natural 2-D system with outstanding physical and electrical properties [1], including evidence of the quantized Hall effect (QHE) at room temperature. This material's unique 2-D magnetotransport properties for quantized Hall resistance (QHR) standards equal or surpass the existing technology based on 2-D transport in semiconductor heterostructures and MOSFET devices [2], [3]. Because of the linear conical band structure near the Dirac points resulting from the hexagonal reciprocal lattice, carriers in graphene mimic relativistic Dirac particles, and conduction is supported for either electrons or holes. An anomalous QHE is observed in a strong magnetic field such that these carriers in monolayer graphene occupy Landau levels with energies that scale as the square root of the magnetic field. The separation of the levels is particularly large between the $n = (0, \pm 1)$ states in monolayer graphene, allowing the QHR plateau with resistance $R_H = h/2e^2$ to be quite robust [4].

Manuscript received July 4, 2012; revised September 2, 2012; accepted September 5, 2012. Date of publication January 15, 2013; date of current version May 8, 2013. The Associate Editor coordinating the review process for this paper was Thomas Lipe.

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Digital Object Identifier 10.1109/TIM.2012.2225962

The unique aspects of graphene's electronic states represent a theoretically important picture that may lead to a basic understanding of the stability of QHE plateaus while enabling a more advanced standard in which the QHE persists at higher currents and temperatures than in other 2-D materials. For some national measurement laboratories, where strict international guidelines [5] for measurement conditions, treatment of devices, and electrical transport characteristics are used, graphene devices may soon be the benchmark of QHR metrological quality.

II. Epitaxial Growth Process

The epitaxial growth process on semi-insulating SiC is particularly suited to QHR device production since it can produce large-scale monolayer graphene directly on an electrically insulating substrate [6], [7]. Unlike in some other processes, e.g., CVD or exfoliated graphene, postproduction transfer to an appropriate substrate is avoided. On surfaces roughly parallel to the hexagonal-symmetry basal plane of 4H-SiC or 6H-SiC polytype samples, graphene self-organizes at extreme temperatures as Si sublimates. In the process we describe here, these 6H-SiC substrates naturally develop 0.75-nm-high steps at temperatures between about 1200 °C and 1500 °C due to the small miscut angle (0°–0.5°) relative to the basal plane. At higher temperatures, these steps transform into terraces through step bunching, a self-limiting process that lowers the chemical potential of the surface.

Extended regions of few-layer epitaxial graphene (EG) can be grown on the Si face, or SiC(0001) surface [8], [9], while irregular graphene regions of different layer numbers and relative orientation are produced on the opposite C-face, or SiC(000-1) surface [10], [11]. The graphene structure in EG (Si face) is created by the initial growth of a covalently bonded buffer layer (BF). This carbon layer is nonconductive due to partial sp^3 hybridization with Si atoms and orients itself in registry with the crystalline structure of the Si face. The BF does, however, induce strong negative doping in EG, and the resulting high carrier concentration disrupts the QHE, so doping control during or after process stages will be required.

The true conductive EG layer consisting of sp^2 bonded carbon atoms forms by a lifting process as a new BF grows [12]. These processes are aided by carbon diffusion at the SiC surface. As shown in Fig. 1, at high temperature, the partial pressure of the dominant Si-containing species in equilibrium with 6H-SiC increases rapidly. Suppression of the diffusion of Si vapor can reduce the rate of BF formation, allowing better control

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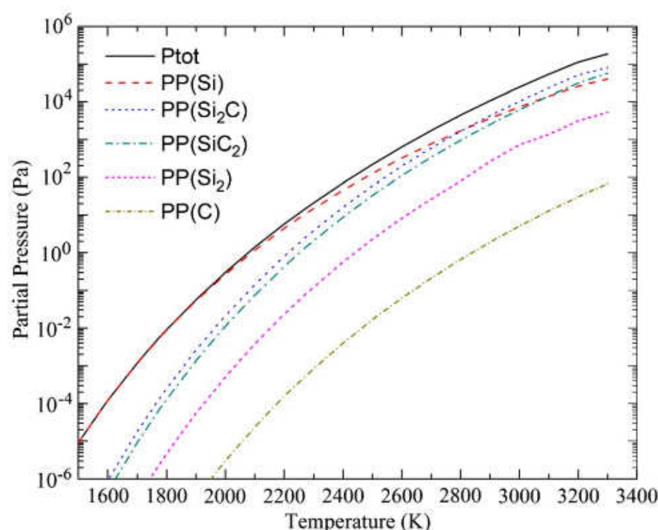

Fig. 1. Equilibrium partial pressure above a bare 6H-SiC surface, calculated using ThermoCalc®.[1] Note that Si and Si_2C are the dominant vapor species, which results in the incongruent sublimation of silicon carbide and formation of graphene layers.

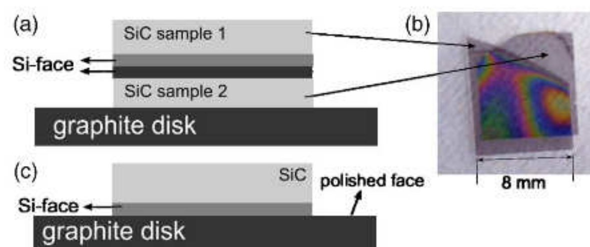

Fig. 2. Disposition of samples in the furnace for annealing: (a) Side view of samples in the FTF method. Both Si faces (darker areas between samples) are facing each other, with the bottom sample resting on a graphite disk which is in contact with a graphite platform. (b) Optical image of two samples placed over each other as in the growth processing step. Note that Newton's rings are visible due to the air-gap interference of fluorescent light. (c) Side view of the disposition in the case of the FTG method, where the sample's Si face is placed against the polished face of a graphite disk. Interference fringes are also visible and are used where possible to position the samples for uniform gap spacing over most of the sample surface.

at higher temperatures [13] where carbon can readily diffuse on the SiC surface. As in [14]–[16], we control the Si sublimation/diffusion rate during annealing at very high temperature by using Ar background gas and by physical confinement, both of which lower the sublimation rate. The Si-rich decomposition products are confined in our laboratory by creating a narrow gap region through which the vapor must diffuse [17], [18]. Suppression of the sublimation rate of silicon species is also known to slow the nucleation process, such that graphene forms at higher temperatures, with larger domains and fewer lattice defects, thus improving the large-scale 2-D device transport characteristics for metrology applications.

We describe a systematic study of EG growth on the SiC(0001) surface by controlled sublimation methods similar to the face-to-face (FTF) method developed in [18] and the face-to-graphite (FTG) method used with SiC(000-1) in [17]. The sample surface structure and the ambient conditions of the annealing process both contribute to the eventual graphene morphology and electronic properties. The electronic properties of graphene can be studied directly and in microscopic detail. The full development of QHE devices presents many technical challenges, i.e., control of the number of graphene layers [4], graphene–metal contacting [19], and equalization of carrier density over large areas [20].

Our complete epitaxial growth process combines most or all of the following steps.

1) The EG layers are grown on the chemically–mechanically polished (CMP) Si face of diced semi-insulating 6H-SiC wafer samples [Abrasifs Grains et Pouders (AGP, Ltd.[1])]. Prior to processing, samples are prepared using a standard cleaning process (see the Appendix).
2) The FTF samples are positioned with the Si face either up or down, facing another bare or previously graphitized 6H-SiC sample of similar size [Fig. 2(a)], while FTG samples are annealed with the Si face down, facing a 25-mm polished graphite surface (Fig. 2(c), substrate-nucleated pyrolytic graphite disk from SPI Supplies, Inc.[1]).
3) Dehydration and cleaning [standard cleaning-dehydration (SC-D)] is conducted in the furnace at 500 °C (60 h)–725 °C (12 h) in Ar background gas. No significant differences in surface morphology for these preprocess baking treatments have been seen using atomic force microscopy (AFM).
4) The epitaxial growth process is controlled by annealing in a sequence of temperature ramp and dwell stages.

Our maximum 2000 °C growth temperature is at least several hundred degrees higher than the range reported by most other groups. A significant exception is Virojanadara *et al.* [9], in which Ar ambient background gas is also used but without the FTF/FTG methods. Similar to [9], we have found that our processes do not require a prior H etching to create a highly ordered SiC surface, so that the processing complexity is reduced. The surface covering in the FTF/FTG also protects the sample from contaminating dust deposition.

In the FTF case, two 8 mm × 8 mm samples are placed together with their Si faces touching each other, as in Fig. 2(a). The average gap between the surfaces is at least 1.0 μm due to the flatness error of the polished wafers (determined by interferometric measurements of sample flatness; see Fig. 3). A rough estimate of the actual gap spacing is based on visual inspection of fluorescent light interference fringes in the cavity [Newton's rings; see Fig. 2(b)] and is estimated to be 1–2 μm. To determine the effect of FTF contact pressure, a small additional weight was occasionally added by placing a second graphite disk on top of the two-sample sandwich. No significant changes were observed under this condition. In the FTG method, the Si face is placed against the polished face of a graphite disk; see Fig. 2(c). An optical interference pattern can also be seen in this case, and careful orientation on the surface is used to obtain a similar gap of 1–3 μm between the Si face and the graphite disk.

Processing occurs in a commercial furnace [Materials Research Furnaces (MRF, Inc.[1])] equipped with a 10-cm-inner-diameter 20-cm-tall cylindrical graphite heating element and

[1]Mention of commercial products or services does not imply endorsement by the National Institute of Standards and Technology (NIST) nor does it imply that such products or services are necessarily the best available for the purpose.

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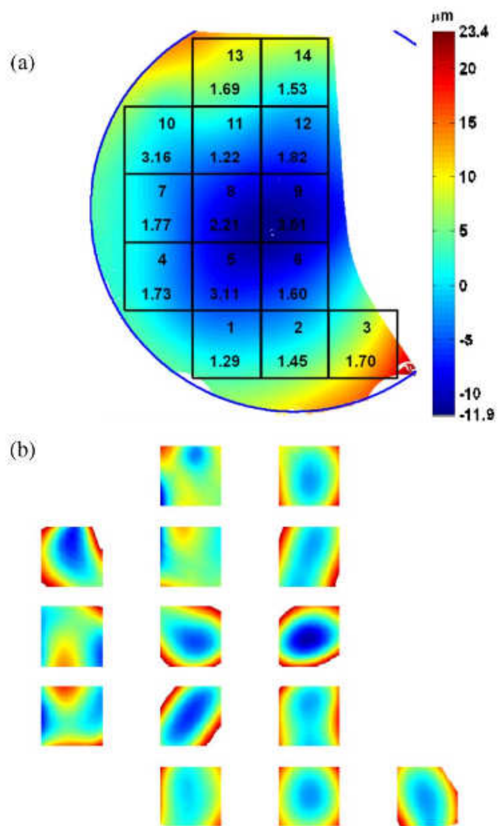

Fig. 3. Laser interferometric measurement of wafer flatness: (a) Section of Si face of a 50-mm SiC wafer, with the measured flatness deviation in false color. Each 8 mm × 8 mm sample area is identified by a sequential number and its peak-to-valley flatness error; (b) flatness deviation of each sample area.

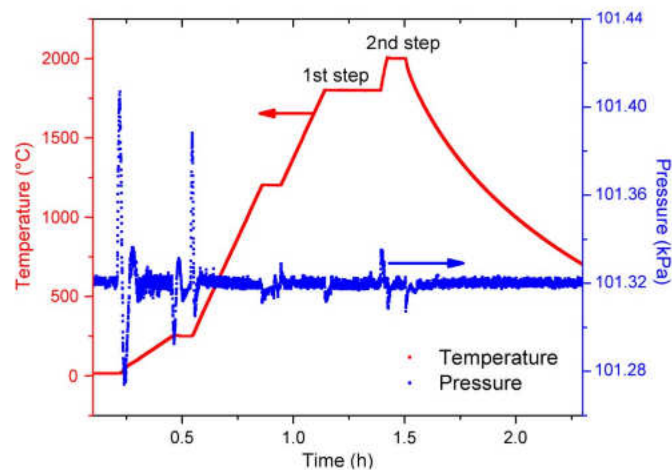

Fig. 4. Example of a temperature and pressure profile during the graphitization process: Brief dwells occur at 250 °C and 1200 °C; BF formation begins at 1800 °C (900 s) followed by a 2000-°C (300 s) step. The overshoot after ramps is < 5 °C, and the temperature stabilizes to ±0.1 °C in less than a minute.

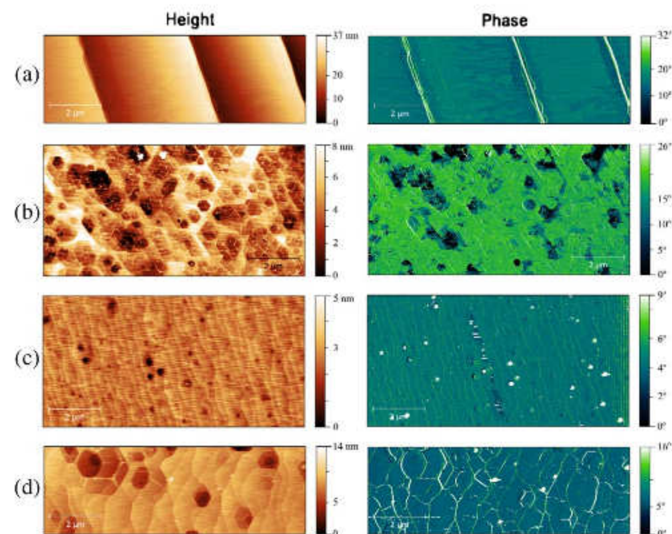

Fig. 5. AFM images (height in nanometers and phase in degrees) of samples; in all cases, the length scale is the same and a single annealing step was used. In (a), annealed at 1750 °C for 2700 s with the FTF method, good step development and phase contrast indicating growth of the BF are observed. Samples shown in (b), (c), and (d) were processed uncapped and open to a 101-kPa Ar background. (b) Annealed at 1750 °C for 2700 s, no steps are obtained, and the surface is highly irregular. (c) Annealed at 1800 °C for 600 s, the surface reconstruction has produced irregular atomic steps but pits are beginning to form. (d) Annealed at 2000 °C for 600 s, a high density of raised pleats indicates advanced graphitization. Note that (b), (c), and (d) all present significant concentrations of surface defects which are absent in the FTF case.

a maximum rated temperature of 2100 °C. The typical process stage temperatures we use are between 1200 °C and 2000 °C with an estimated uncertainty of ±10 °C based on type C thermocouple probes. The uniformity of the sample annealing temperature is better than 10 °C in an 8-cm-diameter region (1.0 °C/8 mm) and is probably improved by annealing the samples in contact with pyrolytic graphite disks. Three commercial temperature and pressure controllers, a mass flow valve for the Ar supply, a butterfly valve, and a roots-type dry pump are used to automatically control the pumping speed and hot zone temperature and pressure. The graph shown in Fig. 4 gives a profile of temperature and pressure versus time as recorded for a complete sample annealing period. In all of the work described here, the background pressure is maintained at 101 kPa ± 0.5 kPa.

III. Results and Discussion

The FTF or FTG methods are crucial in our system since we rely on confinement by the surface covers and diffusion limiting through inert (Ar) background gas to control both surface morphology and graphene growth. Most samples grown uncapped above 1750 °C in our furnace have undesirable surface reconstruction, i.e., the regular terrace development is not obtained and pitting is widespread. Typically, for a wide range of process parameters with the FTF or FTG methods, a large central area of the sample is covered by terraces of uniform widths of 2–6 μm as shown in the AFM images in Fig. 5(a). Samples grown with uncapped processing, as shown in Fig. 5(b)–(d), may have surface morphology with clear atomic steps (0.75-nm height in 6H-SiC) or irregular terraces, but a high density of surface pits develops and is thought to diminish the electrical transport quality of the sample.

Annealing in Ar using either of our methods typically results in BF formation at 1500 °C–1800 °C, with much longer annealing times required at the lower end of this temperature range. Many of our samples were processed with a second annealing step at 1900 °C–2000 °C for 300 s. This causes little further

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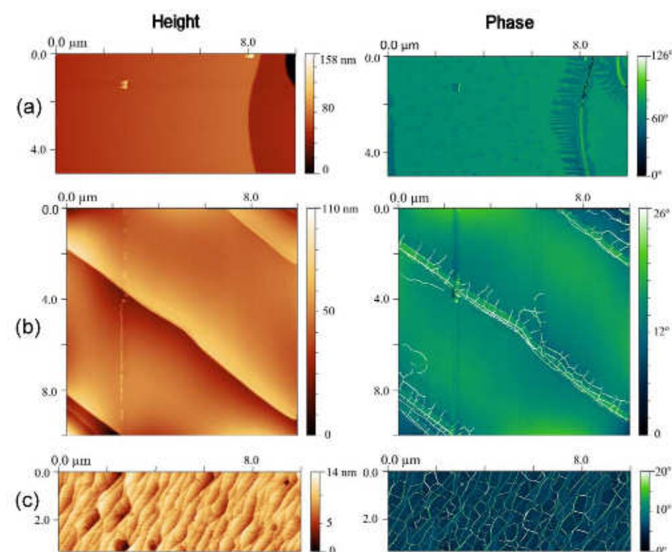

Fig. 6. AFM measurements showing (left) height measurements and (right) phase measurements. (a) Sample grown with FTF annealing at 1800 °C with a 900-s dwell showing "fingers" near the edge of the SiC-substrate atomic terraces that are believed to be a stage of BF development. (b) Sample annealed with a two-step FTF thermal process, adding a dwell of 300 s at 2000 °C to the 1800-°C 900-s process; the white lines in the phase measurement are pleats in the top EG layer(s) indicating more advanced graphitization at the terrace edges. (c) Sample that shows thicker graphitization due to processing described in (b) with no second wafer in contact, i.e., the SiC(0001) surface was exposed to the Ar environment; notice that the pleats cover the whole surface and terraces are not well defined.

terrace development but more advanced EG layer development. The FTG method acts similarly to the FTF method. The main difference between the methods is a larger terraced area in samples grown by the FTG method; in this case, approximately 95% of the sample surface presents well-formed terrace structure and EG growth is thus more uniform.

Fig. 6 shows AFM images of three samples representing different stages of EG layer growth, from the formation of a covalently bound BF to the development of primarily monolayer graphene and finally to a surface covered with multilayer graphene. The last sample was processed open to Ar background, as in Fig. 5(d), so the partial pressure of the decomposition products near the SiC surface was much lower.

In our two-sample FTF process, if neither sample has been previously graphitized, the SiC terrace morphology after annealing at $T > 1800$ °C is sometimes very irregular, with a few very wide (50 μm) terraces developing in some areas and with corresponding regions of erosion or terrace growth in the nearby area of the facing sample. A more uniform surface morphology (straight, parallel, and evenly spaced SiC terraces) is usually obtained if the facing sample has been previously processed to obtain significant graphene layer coverage. This may be because the top sample is exposed to direct radiative heating and the bottom sample is in contact with an initially cooler graphitic surface. Within the gap, a high density of Si- and C-containing species in the vapor phase may initiate mass transfer from one sample to the other, resulting in unstable growth in the terrace formation process of the cooler sample. Presumably, SiC mass transfer due to differences in the temperatures of the top and bottom samples is favored over graphene formation when both surfaces have bare SiC surfaces.

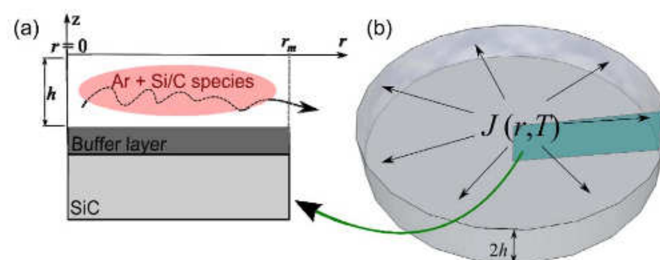

Fig. 7. Geometry of the problem. $J(r;T)$ is the gas flux, r the radial distance, r_m is the maximum radius, T is the temperature, and $2h$ is the gap height. (a) Cross section as indicated, after the BF growth, (b) we assume a cylindrical geometry for the gas to diffuse. Image dimensions are not to scale (r_m ≈ 4 mm; h ≈ 1 μm).

A. Diffusion Model

In this section, we describe a model for the FTF/FTG graphene growth kinetics. We assume that the Si-rich decomposition products undergo two distinct consecutive diffusive processes: atomic diffusion through graphitic surface layers followed by Si vapor diffusion in the Ar-filled gap.

1) At first, the diffusion of sublimated by-products in the Ar-filled gap of height $2h$ between the samples (or sample and graphite) is associated with the BF formation step of epitaxial growth. We assume that all the sublimated Si enters the gap volume directly as the first carbon layer (BF) is formed. Then, the Si vapor diffuses to the edge of the gap and escapes into the much larger furnace volume. Thus, the BF formation is controlled by vapor kinetics, and we calculate that this requires a radial diffusivity constant D_g in the gap on the order of 10^{-3}–10^{-4} $m^2 \cdot s^{-1}$. A Monte Carlo simulation was developed to model the effect of collisions with the surfaces in the gap. Calculations show that, at 1800 °C–2000 °C, the effect of surface collisions can be described by a diffusivity term D_{gs}, with $D_{gs}/2h = (0.56 \times 10^3$ m/s $\pm 0.05 \times 10^3$ m/s). The diffusivity in Ar is 0.6×10^{-3} m^2/s, and thus, the contribution of D_{gs} does not include a significant effect in our model for gaps greater than about 1 μm according to our simulations.
2) Diffusion of Si across the BF or the BF plus one or more layers of EG allows progressive EG growth. In order to match the observed rates of graphene growth, we assume a solid-state diffusivity D_G in the z-direction between 10^{-12} and 10^{-14} $m^2 \cdot s^{-1}$. The kinetic process is controlled by the Si vapor concentration profile in the gap, which drives the diffusion through the carbon layers as well as the radial vapor-state diffusion through the gap.

Fig. 7 shows the geometry proposed to solve the radial diffusion problem for the gas that fills the gap, for which we assume rotational symmetry. If $\rho(r)$ is the Si concentration at distance r from the center of the sample, then the diffusion of Si atoms through the carbon layer with flux $\varphi(r)$ can be described by the following equations:

$$\frac{d^2}{dr^2}\rho(r) = -\frac{D_G}{D_g h \delta}\left[\rho_{eq} - \rho(r)\right] \quad (1)$$

$$\varphi(r) = D_G \frac{\rho_{eq} - \rho(r)}{\delta}. \quad (2)$$

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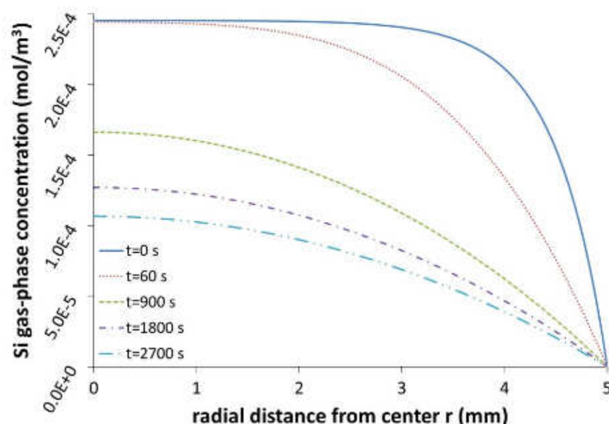

Fig. 8. Plot of the time-dependent solutions of (3) at five points in time for annealing at T = 1900 °C, as described in the text.

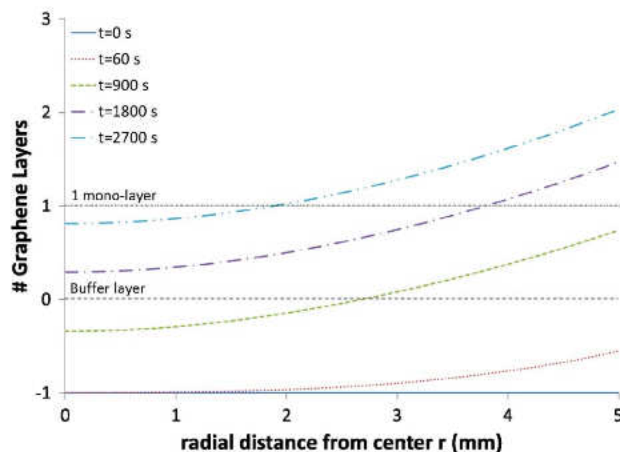

Fig. 9. Plot of the time-dependent solutions for the graphene layer coverage, with a bare SiC surface being □1, at five points in time and an annealing temperature T = 1900 °C, as described in the text.

Here, ρ_{eq} is the calculated equilibrium concentration value for Si from Fig. 1, and δ is the carbon layer thickness. The equilibrium radial concentration condition at a given temperature is reached by continuous diffusion through the carbon layer. The solution of these equations for the simpler 1-D problem is

$$\rho(r) = \rho_{eq}\left[1 - A(b, r_m)\cosh(b \cdot r)\right] \tag{3}$$

where A is a constant that depends on the sample radius r_m and $b = (D_G/D_g h\delta)^{1/2}$. The 2-D problem solution is given by a linear combination of Bessel functions. For the boundary conditions, we assume that $d\rho(0)/dr = 0$ and $\rho(r_m) = 0$. Fig. 8 shows graphs of the solutions for annealing at $T = 1900$ °C for 2700 s, with $D_g = 1 \times 10^{-3}$ $\mathrm{m^2 \cdot s^{-1}}$, $D_G = 2 \times 10^{-13}$ $\mathrm{m^2 \cdot s^{-1}}$, $\rho_{eq} = 2.45 \times 10^{-4}$ $\mathrm{mol \cdot m^{-3}}$, $r_m = 5$ mm, and $2h = 2.5$ μm.

The layer thickness δ is allowed to vary continuously as $\delta(r)$ and is calculated at the end of each time period. The results of the 2-D growth calculations shown in Fig. 9 represent this statistical distribution of graphene layers. They simulate the increase in graphene coverage in each time period; based on the Si concentration profile and layer distribution found for the previous time period, a 5 s step time was used in this case. The Si-rich vapor can more easily escape closer to the edges, and the resulting lower Si concentration allows graphene to grow only near the sample edges initially. The growth extends toward the sample center over longer times as the Si gas-phase concentration decreases near the center. The layer profiles shown in Fig. 9 become more uniform with time since extra graphene coverage lowers the sublimation rate at the edges than near the center.

Surface analysis techniques have been used to determine the extent of graphitization on our samples. AFM is routinely performed on all samples, and coverage can be roughly gauged by the observation of phase contrast and characteristic step height changes and by pleatlike folds in the case of multilayer graphene. Ellipsometry has been used to identify the transition from SiC to BF. Micro-Raman measurements at 514.5 nm verify the presence of EG layers and can be used to identify disorder and layer thickness from peak shapes and positions. Raman measurements also have identified a transition from BF to a quasi-free-standing graphene monolayer in some samples subjected to hydrogen intercalation processing. Finally, low-energy electron microscopy (LEEM) and related techniques give quantitative data on the number of layers. For example, LEEM indicates that primarily monolayer EG was formed over a large central region of an FTG sample processed at $T =$ 1900 °C for 1800 s. Our preliminary results indicate that a range of temperatures between about 1800 °C and 2000 °C may produce uniform graphene growth that can be controlled to produce monolayer EG with desirable electronic properties.

IV. Conclusion

We have been developing a reliable process to create large-domain graphene on semi-insulating SiC substrates for metrology applications. Both terrace formation and the rates of SiC decomposition can be controlled at temperatures of 1600 °C–2000 °C by increasing the concentration of Si-containing species at the solid–vapor interface. Using the FTF and FTG methods, the diffusion rate is reduced by confining the vapor in a gap between a SiC(0001) surface and a second parallel surface in close contact. We find that this inhibits Si sublimation so that the graphene layer formation is uniform and controlled. While we do not obtain terrace steps for sample surfaces exposed directly to background Ar gas at 101 kPa, terraces form over 95% of the sample surface when a CMP polished SiC(0001) surface is processed facing polished graphite and over 50%–80% of the surface when heating occurs facing a pregraphitized SiC surface. In our system, samples open to the environment develop several EG layers at 1800 °C–2000 °C. These results indicate that very high temperatures are not readily applicable for monolayer EG growth without the FTF/FTG methods, even at a 101-kPa Ar background pressure.

We have modeled the process to study the formation conditions required for both BF and first EG layer coverage. In our methods, two distinct processes are involved. SiC substrate terraces develop, and a BF forms with rapid outward diffusion of Si/C species through the surface-to-surface gap, and the first EG layer is obtained with the added constraint of diffusion of Si-bearing vapor in the z-direction through the BF. This second process is limited by a diffusivity roughly ten orders of magnitude lower than that for diffusion in the Ar-filled gap.

Stepwise calculations assuming kinetic equilibrium between gap vapor concentration and the two diffusion processes allows the calculation of the BF and EG layer thickness as a function of time and temperature. We find that the model describes the growth process qualitatively and is in good agreement with the experimental results for reasonable values of the diffusion constants.

Appendix

The samples were cleaned using the following standard cleaning process:

1) Industrial soap cleaning.
2) Hot solvent sequence: Samples are immersed sequentially in heated trichloroethylene, acetone, isopropyl alcohol, and deionized water (DIW).
3) Cleaned in room-temperature concentrated hydrofluoric acid (HF) solution for 30 s and immediately washed in DIW and blowing dry with N_2.

It is noteworthy that the cleaning and baking process does not always lead to well-formed terrace morphology in the FTF method, particularly when two bare SiC samples are graphitized at the high end of the temperature range. Silicon carbide samples may undergo extensive mass transfer prior to graphitization, sometimes forming nearly mirror-image surface features, or the processing may lead to the development of deeply etched pits. In placing and removing the samples in the water-jacketed top-loading furnace, the Ar flux is increased to 5000 standard cm^3/min, and the furnace is not opened until the interior temperature is below room temperature. In this way, the graphite lining of the furnace suffers minimal exposure to air, which might increase the reactivity of the SiC surface.

Acknowledgment

The authors would like to thank Prof. R. Feenstra (Carnegie Mellon University), I. Calizo of the National Institute of Standards and Technology (NIST) (now at Florida International University), and A. Boosalis (University of Nebraska—Lincoln), as well as A. Hight-Walker, B. Bush, S. Krylyuk, and U. Griesmann of NIST. Official contribution of NIST, not subject to copyright in the U.S.

References

[1] A. H. Castro-Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan.–Mar. 2010.

[2] T. Janssen, N. E. Fletcher, R. Goebel, J. M. Williams, A. Tzalenchuk, R. Yakimova, S. Kubatkin, S. Lara-Avila, and V. I. Falko, "Graphene, universality of the quantum Hall effect and redefinition of the SI system," *New J. Phys.*, vol. 13, no. 9, p. 093026, Sep. 2011.

[3] F. Delahaye, D. Dominguez, F. Alexandre, J. P. Andre, J. P. Hirtz, and M. Razeghi, "Precise quantized Hall resistance measurements in GaAs/$Al_xGa_{(1-x)}As$ and $In_xGa_{(1-x)}As$/InP heterostructures," *Metrologia*, vol. 22, no. 2, pp. 103–110, Jan. 1986.

[4] A. Tzalenchuk, S. Lara-Avila, A. Kalaboukhov, S. Paolillo, M. Syväjärvi, R. Yakimova, T. J. B. M. Janssen, S. Kopylov, V. Fal'ko, and S. Kubatkin, "Towards a quantum resistance standard based on epitaxial graphene," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 186–189, Mar. 2010.

[5] F. Delahaye and B. Jeckelmann, "Revised technical guidelines for reliable DC measurements of the quantized Hall resistance," *Metrologia*, vol. 40, no. 5, pp. 217–223, Oct. 2003.

[6] J. Jobst, D. Waldmann, F. Speck, R. Hirner, D. K. Maude, T. Seyller, and H. B. Weber, "Quantum oscillations and quantum Hall effect in epitaxial graphene," *Phys. Rev. B, Condens. Matter*, vol. 81, no. 19, p. 195434, May 2010.

[7] S. Lara-Avila, A. Tzalenchuk, S. Kubatkin, R. Yakimova, T. J. B. M. Janssen, K. Cedergren, T. Bergsten, and V. Fal'ko, "Disordered Fermi liquid in epitaxial graphene from quantum transport measurements," *Phys. Rev. Lett.*, vol. 107, no. 16, p. 166602, Oct. 2011.

[8] W. Lu, J. J. Boeckl, and W. C. Mitchel, "A critical review of growth of low-dimensional carbon nanostructures on SiC (0001): Impact of growth environment," *J. Phys. D, Appl. Phys.*, vol. 43, no. 37, p. 374004, Sep. 2010.

[9] C. Virojanadara, M. Syväjarvi, R. Yakimova, and L. I. Johansson, "Homogeneous large-area graphene layer growth on 6H-SiC(0001)," *Phys. Rev. B, Condens. Matter*, vol. 78, no. 24, p. 245403, Dec. 2008.

[10] J. Hass, F. Varchon, J. E. Millán-Otoya, M. Sprinkle, N. Sharma, W. A. de Heer, C. Berger, P. N. First, L. Magaud, and E. H. Conrad, "Why multilayer graphene on 4h-SiC(000 $\bar{1}$) behaves like a single sheet of graphene," *Phys. Rev. Lett.*, vol. 100, no. 12, p. 125504, Mar. 2008.

[11] Luxmi, N. Srivastava, G. He, R. M. Feenstra, and P. J. Fisher, "Comparison of graphene formation on C-face and Si-face SiC {0001} surfaces," *Phys. Rev. B, Condens. Matter*, vol. 82, no. 23, p. 235406, Dec. 2010.

[12] W. A. de Heer, C. Berger, M. Ruan, M. Sprinkle, X. Li, Y. Hu, B. Zhang, J. Hankinson, and E. Conrad, "Large area and structured epitaxial graphene produced by confinement controlled sublimation of Silicon Carbide," *Proc. Nat. Acad. Sci. USA*, vol. 108, no. 41, pp. 16 900–16 905, Oct. 2011.

[13] J. B. Hannon, M. Copel, and R. M. Tromp, "Direct measurement of the growth mode of graphene on SiC(0001) and SiC(000-1)," *Phys. Rev. Lett.*, vol. 107, no. 16, p. 166101, Oct. 2011.

[14] C. Virojanadara, M. Syväjarvi, A. A. Zakharov, T. Balasubramanian, R. Yakimova, and L. I. Johansson, "Morphology characterization of argon-mediated epitaxial graphene on C-face SiC," *Phys. Rev. B, Condens. Matter*, vol. 78, no. 24, p. 245403, Dec. 2008.

[15] K. V. Emtsev, A. Bostwick, K. Horn, J. Jobst, G. L. Kellogg, L. Ley, J. L. McChesney, T. Ohta, S. A. Reshanov, J. Röhrl, E. Rotenberg, A. K. Schmid, D. Waldmann, H. B. Weber, and T. Seyller, "Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide," *Nature Mater.*, vol. 8, no. 3, pp. 203–207, Mar. 2009.

[16] M. Real, T. Shen, G. R. Jones, R. E. Elmquist, J. A. Soons, and A. Davydov, "Graphene epitaxial growth on SiC(0001) for resistance standards," in *Proc. CPEM*, Jul. 2012, pp. 600–601.

[17] N. Camara, J.-R. Huntzinger, G. Rius, A. Tiberj, N. Mestres, F. Pérez-Murano, P. Godignon, and J. Camassel, "Anisotropic growth of long isolated graphene ribbons on the C face of graphite-capped 6H-SiC," *Phys. Rev. B, Condens. Matter*, vol. 80, no. 12, p. 125410, Sep. 2009.

[18] X. Yu, C. Hwang, C. M. Jozwiak, A. Kohl, A. K. Schmid, and A. Lanzara, "New synthesis method for the growth of epitaxial graphene," *J. Electron Spectrosc. Relat. Phenom.*, vol. 184, no. 3–6, pp. 100–106, Apr. 2011.

[19] V. K. Nagareddy, I. P. Nikitina, D. K. Gaskill, J. L. Tedesco, R. L. Myers-Ward, C. R. Eddy, J. P. Goss, N. G. Wright, and A. B. Horsfall, "High temperature measurements of metal contacts on epitaxial graphene," *Appl. Phys. Lett.*, vol. 99, no. 7, p. 073506, Aug. 2011.

[20] S. Lara-Avila, K. Moth-Poulsen, R. Yakimova, T. Bjørnholm, V. Fal'ko, A. Tzalenchuk, and S. Kubatkin, "Non-volatile photochemical gating of an epitaxial graphene/polymer heterostructure," *Adv. Mater.*, vol. 23, no. 7, pp. 878–882, Feb. 2011.

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Eric A. Lass, photograph and biography not available at the time of publication.

Fan-Hung Liu, photograph and biography not available at the time of publication.

Tian Shen, photograph and biography not available at the time of publication.

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