Graphene Epitaxial Growth on SiC(0001) for Resistance Standards

Mariano A. Real[1,2], Tian Shen[1], George R. Jones[1], Randolph E. Elmquist[1], Johannes A. Soons[1], and Albert V. Davydov[1]

[1]National Institute of Standards and Technology, Gaithersburg, MD 20899, USA
[2]Instituto Nacional de Technología Industrial, San Martín, Buenos Aires, Argentina
mreal@inti.gob.ar

***Abstract* — Epitaxial growth of graphene layers on 6H-SiC(0001) substrates are studied to improve the performance of graphene for metrological applications. A face-to-face (FTF) annealing method at 2000 °C in an Ar background atmosphere are used to inhibit the rates of SiC decomposition and Si sublimation and thus control the graphene layer development. Sample surface morphology and its relation to changes in the growth conditions are described.**

***Index Terms* — Electrical resistance standards, epitaxial growth, graphene, surface morphology, quantum Hall effect.**

I. Introduction

Graphene is a natural two-dimensional (2D) system which makes possible the development of a quantum Hall resistance (QHR) standard based on a new technology. Given the special nature of its reciprocal lattice, carriers mimic Dirac particles and an anomalous quantum Hall effect (QHE) [1] can be observed. The epitaxial growth process on 6H-SiC(0001) is a proven approach to realize graphene-based devices with metrological QHR characteristics [2] and is particularly suited to obtaining large-scale pristine graphene directly on an electrically-insulating SiC substrate without transfer. This method presents several technical challenges, i.e. control of the number of graphene layers, graphene-metal contacting, and equalization of carrier density over large areas.

II. Epitaxial Growth Process

We describe a systematic study of epitaxial graphene growth on the SiC(0001) surface by a sublimation method, similar to the "face-to-face" (FTF) method developed in [3]. The sample morphology is intimately related to the growth conditions, so by controlling the growth we aim to find a reliable process to obtain samples suitable for metrology applications. The epitaxial graphene layers are grown on the chemically-mechanically polished (0001) face of semi-insulating SiC wafers in an Ar atmosphere. Processing occurs in a commercial furnace equipped with a 10 cm inner diameter, 20 cm tall cylindrical graphite heating element. In all cases the background pressure was maintained at 101.32 kPa with 300 standard cm^3/min Ar flow rate.

Our complete epitaxial growth process combines treatment of diced SiC wafer samples with some or all of the following steps: i) cleaning in concentrated HCl solution at most one hour prior to introduction to the furnace, ii) dehydration and cleaning at 500 °C for 60 h in Ar background gas, iii) H_2-etching with 4% H_2/Ar gas mixture, and iv) graphene epitaxial growth at temperatures up to 2000 °C. The growth temperature is several hundred degrees higher than the range reported by most other groups [3] - [4] and, together with the high Ar ambient background pressure, duplicates the ambient conditions reported in [2]. Higher growth temperatures and ambient Ar background pressure should favor fewer graphene nucleation centers and larger single-crystal domain coverage.

Steps ii) and iii) are made with samples separated from each other to avoid water or impurities being trapped between them. It is noteworthy that any accidental contact of SiC samples with laboratory air between steps ii) and iv) may lead to the development of etching pits. Since the samples are placed face to face before step iv) and the furnace must be open for FTF sample placement, the Ar flux is increased to 5000 standard cm^3/min and the top-loading furnace is not opened until the temperature is below room temperature. In this way the samples are not exposed to air.

Usually two 8 mm × 8 mm samples are placed together with their Si-faces touching each other, as in Fig. 1a). The average gap between the surfaces is several tenths of a micrometer due to the flatness error and residual roughness of the epi-ready polished wafers, and possible particle contamination. This rough estimate is based on visual inspection of fluorescent light interference fringes in the cavity (see Fig. 1b) and interferometric measurements of sample flatness.

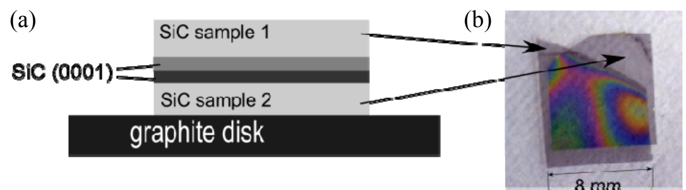

Fig. 1. (a) Side view of the disposition of samples in the furnace. Both Si-faces (darker areas between samples) are facing each other, with the bottom sample resting on a graphite disk which is in contact with a graphite platform. (b) Optical image of two samples placed over each other as in the growth processing step. Note that Newton's rings are visible due to the air-gap interference of fluorescent light.

B. Process conditions and results

We have studied sample morphology and graphene layer coverage after growth in different scenarios: a) with and without previous H_2-etching at 1600 °C with a 4 % H_2/Ar

mixture, b) with and without prior HCl solution cleaning, and c) with growth at two sequential temperature steps, the first at 1800 °C (900 s) and the second at 2000 °C (300 s), of which each have also been used alone. To determine the effect of contact pressure, additional weight was occasionally added by placing a second graphite disk on top of the two-sample sandwich.

Samples were also used with a pattern of 0.25 mm circular mesas developed before the growth process. The patterning reduces the gaps between the mesa surfaces and the opposing polished SiC face by decreasing the effects of wafer flatness errors.

After the growth, graphene layers were studied by atomic force microscopy (AFM) and other microscopy methods. At 1800 °C, 900 s of epitaxial growth typically results in the initial stages of buffer layer formation, while additional growth at 2000 °C for 300 s yields more advanced graphene layer development.

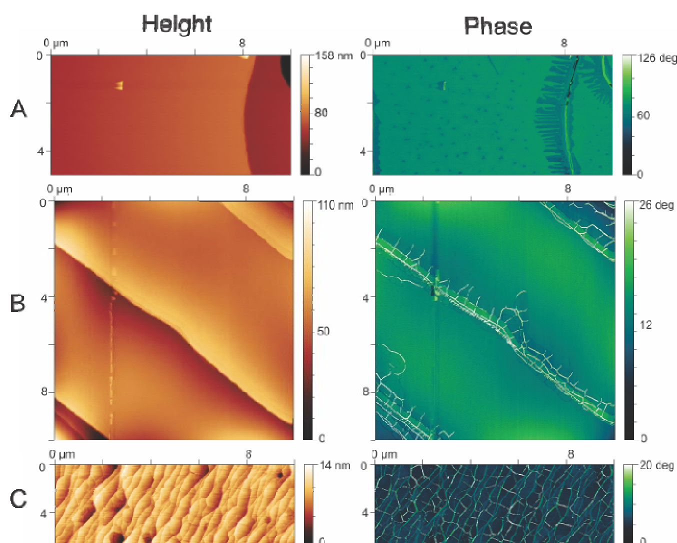

Fig. 2 AFM measurements, showing (*left*) height measurements and (*right*) phase measurements. (A) Sample grown without the final 2000 °C dwell showing "fingers" near the edge of the SiC-substrate atomic terraces that are the initial stages of buffer layer development. (B) Sample grown with the full thermal process; the white lines in the phase measurement are pleats in the top graphene layer. (C) A sample that shows thicker graphitization due to full processing with no second wafer in contact, i.e., the SiC(0001) surface was exposed to the Ar environment; notice that the pleats cover the whole surface.

Figure 2 shows AFM images of three samples representing different stages of graphene layer growth, from formation of a covalently bound buffer layer, to development of primarily monolayer graphene, and finally to a surface covered with multilayer graphene. The last sample was processed open to Ar background, so the pressure of the decomposition products near the SiC surface was much lower. In this case, the only external constraint on the escape of these products is provided by collisions with the Ar background gas.

In our 2-sample sandwich design one sample usually develops better graphene layer morphology, i.e. fewer pleats and straighter SiC steps in the case of no previous H-etching, if the other sample has been previously processed to obtain significant graphene layer coverage. When neither sample has been previously graphitized, the SiC terrace morphology is much less uniform. This difference may be due to temperature gradients between the top and bottom samples inducing transfer of Si- and C- containing species in the vapor phase from one sample to the other

III. Conclusion

We are developing a reliable process to obtain pristine graphene on semi-insulating SiC substrates for metrology applications. An exhaustive study of the growth process is being made, in which an FTF sublimation method is used to reduce the rate of SiC thermal decomposition. As described in [4] and [5], it is crucial to control the decomposition rate at high temperatures by increasing the partial pressure of Si-containing species at the solid-vapor interface. This increase occurs naturally between the two samples, inhibiting Si sublimation so that the graphene layer formation is uniform and controlled. SiC surface cleaning and avoidance of direct contact of the clean sample with air inhibits gross surface reconstruction which otherwise results in poor graphene layer formation. Surface morphology and graphene layer identification through AFM, scanning electron microscopy (SEM), and other methods will be presented.

Acknowledgement

The authors wish to thank Professor Randall Feenstra of Carnegie-Mellon University, Eric Lass of NIST, and Ulf Griesmann of NIST for many helpful discussions.

References

[1] A.H. Castro-Neto, F. Guinea, N.M.R. Peres, K.S. Novoselov and A.K. Geim, "The electronic properties of graphene", *Rev. Mod. Phys.*, **81** (1), pp 109-162, 2010.

[2] T. Janssen, N.E. Fletcher, R. Goebel, J.M. Williams, A. Tzalenchuk, R. Yakimova, S. Kubatkin, S. Lara-Avila and V.I. Falko, "Graphene, universality of the quantum Hall effect and redefinition of the SI system", *New Journal on Physics*, vol. 13, p. 093026, 2011.

[3] X.Z. Yu, C.G. Hwang, C.M. Jozwiak, A. Kohl, A.K. Schmid and A. Lanzara, "New synthesis method for the growth of epitaxial graphene", *J. Electron. Spectrosc. Relat. Phenom*. vol. 184, pp.100-106, 2011.

[4] J.L. Tedesco, G.G. Jermigan, J.C. Culbertson, J.K. Hite, et al, "Morphology characterization of Ar-mediated epitaxial graphene on C-face SiC", *Appl. Phys. Lett.*, vol 96, p. 222103, 2010.

[5] W.A. de Heer, C. Berger, M. Ruan, M. Sprinkle, X. Li, Y. Hu, B. Zhang, J. Hankinson and E. Conrad, "Large area and structured epitaxial graphene produced by confinement controlled sublimation of Silicon Carbide", *P. Natl. Acad. Sci. USA.*, vol. 108 no. 41, pp. 16900-16905, 2011.