TESTING OF A MEMS SOI MICRORELAY

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SUMMARY

In this paper we present the first results of the design, packaging and testing of a MEMS microrelay with lateral contact structures driven by electrostatic actuators. The fabrication of prototypes was made using the surface micromachining process on epitaxied SOI (Epi-SOI) from a MEMS foundry through MPW (Multi Project Wafer) run service.

Twenty-two devices with different structure dimensions were designed in order to evaluate the threshold voltage variation related to geometry. We proposed three microrelay sizes: *small*, *medium* and *large*, defined by its width: 490, 700 and 910 μm, respectively. Active area of prototypes was 3400x3100 μm^2.

Two models of LTCC (Low Temperature Co-fired Ceramics) packaging for the microrelay prototypes were performed: a top contact design with all electrical connections at one side of the packaging, and a bottom contact design using through holes.

A post-processing Ni-Au electroless deposition was realised in order to reduce the lateral contact resistance of microrelays.

The threshold voltage needed to close the microrelay contact was measured for several devices. This voltage was between 25V and 35V for devices *large* and from 30V to 50V for devices *medium*. For devices *small* a displacement was observed with a voltage from 50V to 80V, but they did not close completely.

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ABSTRACT

In this paper we present the first results of the design, packaging and testing of a MEMS microrelay with lateral contact structures driven by electrostatic actuators. The fabrication of prototypes was made using the surface micromachining process on epitaxied SOI (Epi-SOI) from a MEMS foundry through MPW (Multi Project Wafer) run service.

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1. INTRODUCTION

The fabrication of MEMS (Micro Electro-Mechanical Systems) is based on the well-known VLSI technology. Nowadays there are several foundry services available around the world for MEMS fabrication. Nevertheless, it is difficult to find a full compatible fabrication process for specific designs. There are a lot of different technologies available for MEMS fabrication and only some standard processes are implemented in foundries. On the other hand, SOI technology has proved to be a very good option to apply in microsensors and MEMS development [1]. In that area, microrelays demonstrated to have many advantages related to conventional electro-mechanical relays [2,3].

LTCC (Low Temperature Co-fired Ceramics) tape materials for 3D structures using multi-layer have many benefits for packaging silicon based MEMS components. Cavities structures, in which the MEMS can be bonded and hermetically sealed, and a good match of thermal coefficient of expansion (TCE) between ceramic and Si are some advantages of LTCC technology.

In this paper we present the first results of the design, packaging and testing of a laterally driven electrostatic microrelay using MEMS foundry services. Several devices with different structure dimensions were designed and prototypes were fabricated in order to evaluate the comb drive actuator and its threshold voltage variation. The MPW (Multi Project Wafer) service from Tronic's was used for the prototypes fabrication, with SOI wafers. Two types of LTCC packaging for the microrelay prototypes were performed.

2. DESIGN

The fabrication process based on SOI wafers allowed to obtain the complete design of the devices in only one mask. A parameterised hierarchical structure with the Cadence layout editor was used. Parameterised cells were used to define basic structures, hereafter named “basic cells”. Twenty-two different devices in the active wafer area were made easily through the basic cells, which reduced considerably design time.

Microrelay structure is based on a double-fold spring and a pair of comb drives arranged symmetrically at both sides of the movable lateral contact [4,5]. Fig.1 shows the basic cell of the comb drives, while Fig.2 represents a basic schematic diagram of the microrelay structure.

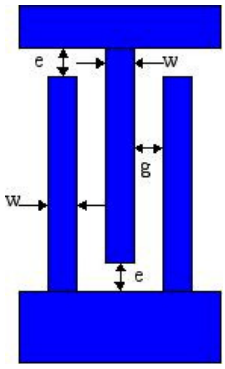

Fig.1: A basic cell to develop the comb drive

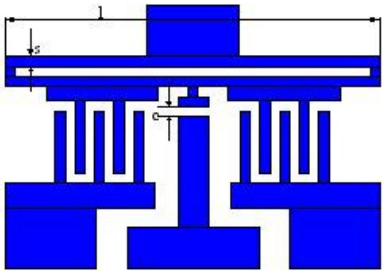

Fig.2: Schematic diagram of a microrelay basic structure

We proposed three microrelay sizes: *small*, *medium* and *large*, defined by its width *l* (490, 700 and 910 µm, respectively). Table1 summarizes the different dimensions of elements that conform the basic cells. The twenty-two devices were arranged in an active area of 3400x3100 μm^2 available in the fabrication process.

Table 1: Main dimensions of devices

Parameters	*Dimensions [µm]*		
l/2	*small*	*medium*	*large*
w	245	350	455
g	3	3	3
e	2.2 - 3	2.2 - 3	2.2 -3
c	2	2	2
s	3	3 - 4	3 - 4
# fingers	10 to 11	11 to 21	11 to 21

The goal of the designed configurations was to study the behaviour of the threshold voltage related to geometry. In order to reduce the threshold voltage we proposed a second microrelay basic structure (Fig.3) looking for an improvement of spring elasticity.

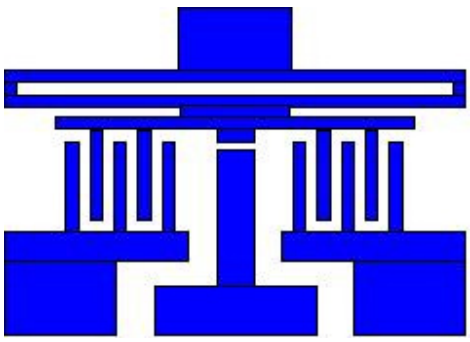

Fig.3: Schematic diagram of a microrelay basic structure - Spring variant

Pads of 200x200µm with 250µm pitch were distributed on two sides around the active area and connected to microrelays. The complete layout of the prototypes is shown in Fig.4.

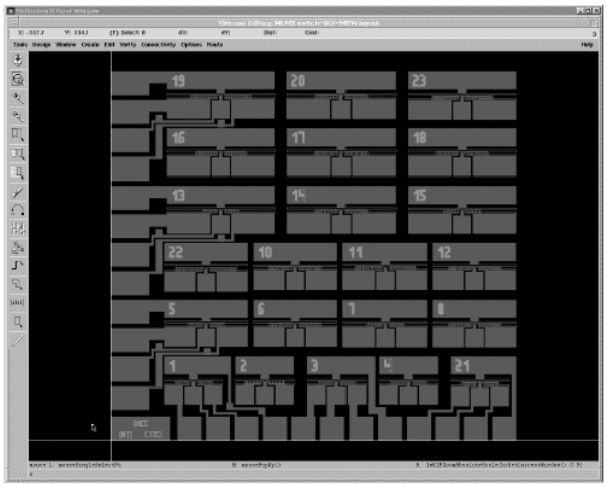

Fig.4: Prototype layout

3. FABRICATION

The fabrication of prototypes was made using the surface micromachining process on epitaxied SOI (Epi-SOI) from TRONIC'S Microsystems through MPW (Multi Project Wafer) run service [6]. The main features of the technology are 20µm thick single crystal silicon active and 0.4µm thick sacrificial layers. The last step of the process is a wafer level packaging to protect structures. This cap was removed by heating the prototypes in a hot plate at 240ºC during 5s. A SEM micrograph of one of the devices is shown in Fig.5.

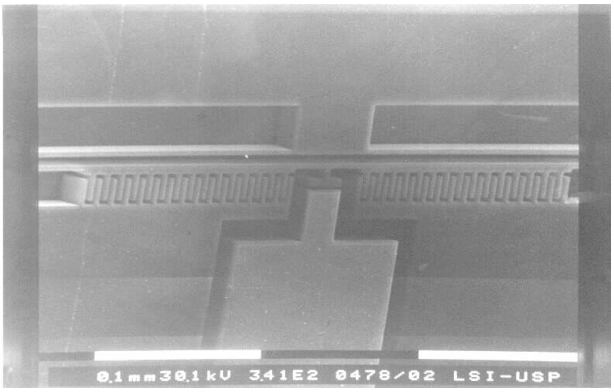

Fig.5 SEM micrograph of one microrelay

In order to reduce the lateral contact resistance of microrelay an additional metal layer was needed. As a metallization of the structure and contact surfaces were not allowed in the fabrication process, a post-processing nickel-gold electroless deposition was realised. Electroless nickel deposition onto silicon surface was done by an activation step in acid solution at 60ºC from 60 to 100 s, followed by 20 minutes annealing at 410ºC [7]. The formed nickel film was from 100 to 160 nm thick. Once silicon surface was covered, the growth of gold film was performed in alkaline solution [8]. In this case, after a 7 minutes immersion the thickness of the gold film was about 100nm. Due to all the structure anchors have an undercut of at least 10µm, electrical contact between structures was avoided.

4. PACKAGING

Low Temperature Co-fired Ceramic (LTCC) is well known as an appropriate material for multilayer packaging. This material joined to thick film technology results in an interesting field for MEMS applications [9,10].

Table 2. Packaging dimensions for both designs

Die's cavity [mm^2]	8 x 8
Connection's cavity [mm^2]	14 x 14
Internal pads: ellipse, [µm^2]	400 x 800
Internal pad's pitch [µm]	750
Connection width [µm]	200

For our MEMS microrelay packaging we proposed two models. The first one was a top contact design, with all electrical connections at one side of the packaging, while the second model was a bottom contact design, using through holes. Table 2 shows general packaging dimensions at green state before co-firing process, for a die size of 4900x4600 µm^2. Table 3 presents the differences between both designs.

Table 3. Specific dimensions for Top and Bottom models

	Top	*Bottom*
External pads [µm^2]	1000x1000	∅ 640
External pad's pitch [µm]	2000	1850
Trough holes [µm]	--	320

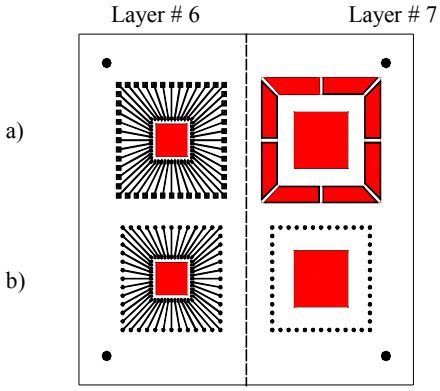

Fig.6: Mask design. a) Top connection b) Bottom connection

Twelve layers were necessary to achieve a properly package and height, with the following sequence

- layer #1-2 die support
- layer #3-5 cavity for die
- layer #6 electrical connections (Fig.6)
- layer #7 pattern for cavities (Fig.6)
- layer #8-12 cavity for wire bonding

DuPont LTCC Green Tape 951 AT and DuPont 6148 silver thick film paste were used, with screen printing technique. Lamination pressure was of 1 kg.mm^{-2}, at 100°C during 3 minutes. After cavities and through holes were done the lamination was cut by dash line. Layers # 7-12 were flipped over layers #1-6 and final lamination was processed. Typical firing procedure for LTCC was applied and a shrinkage value of 14% in x-y direction was obtained.

MEMS microrelay dies were attached to LTCC package with Dow Corning 7920 material. Fig.7 shows first prototypes of MEMS packages obtained with LTCC multilayer ceramic technology.

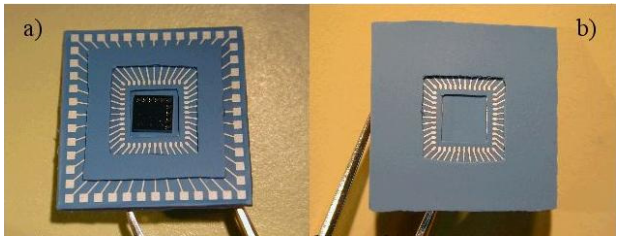

Fig.7: MEMS microrelays prototypes into LTCC package. a) Top connection design. b) Bottom connection design

5. TESTING

Some preliminary tests were performed in a probe station at ambient air before packaging. A Wentworth PML 8000 analytical prober and an Agilent 4156 Semiconductor Parameter Analyser were used. A CC9602 CCD camera allowed recording the displacement of the movable contact.

The threshold voltage needed to close the microrelay contact was measured for several devices. This voltage was between 25V and 35V for devices *large* and from 30V to 50V for devices *medium*. For devices *small* a displacement was observed with a voltage from 50V to 80V, but they did not close completely. When the applied voltage was up to 90V, these types of microrelays were broken due to isolation rupture.

All tests were performed after nickel deposition, so the contact resistance measured in all cases was extremely high. The microrelays behaviour after gold deposition and their lifetime tests are in progress.

The integration of the silicon microrelay into the LTCC package is currently under characterisation at CITEI.

6. CONCLUSION

Electrostatic laterally driven microrelays were designed and fabricated using MPW standard fabrication process on SOI wafers. Twenty-two microrelays were obtained for each prototype with different sizes and actuating structures. Electroless nickel-gold post-processing metallization was made over the structures. Threshold voltage of several devices was measured. The devices were actuated in a relatively low voltage range (25 to 50 V). Two types of LTCC packaging for the microrelay prototypes were performed.

The novelty of the SOI microrelay presented relies on standard processes for fabrication and packaging.

7. ACKNOWLEDGMENTS

This work was partially supported by BID 1201-OC/AR FONTAR project PMT II CAI 064 and CYTED-SP IX Red IX.I-TESEO. The authors would like to thank to M. Bariatto Fontes, H. Furlan and S. Dos Santos Filho from LSI-USP and M. Góngora from IPT-Sao Paolo for their technical support.

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