

Modeling of a Sampling System based on Sigma-Delta ADC for Data Acquisition in Metrology

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Abstract — This paper describes the use of modeling to improve the accuracy of a sampling system built around a Sigma-Delta analog-to-digital converter. The parameters of the model were established using waveforms from a programmable Josephson array. The validation results have shown that the achievable accuracy is within $8 \mu\text{V/V}$ for signals in the frequency range up to 1.3 kHz at equivalent sampling rates below 32 kHz.

Index Terms — Sigma-Delta data converters, analog/digital conversion, modeling, model parameter identification, Josephson voltage standard.

I. INTRODUCTION

Sampling techniques are widely used at National Metrology Institutes (NMIs) in ac metrology applications in order to perform high accuracy measurements. In this work, such a sampling system has been developed with a target uncertainty below $10 \mu\text{V/V}$ [1] for signals in the frequency range up to 1.3 kHz at sampling rate of 8 kHz. In a departure from previous developments at this level of accuracy, deviations in the electronic components chosen for this sampling system have been characterized and are corrected in software in order to reconstruct the signal at its input terminals.

The parameters in the model have been determined using a Josephson Waveform Synthesizer (JWS). The quantum accurate voltages from the JWS render it a noise- and drift-free signal generator for the purposes of this work. Measuring the parameters in the model is equivalent to calibrating the data acquisition system. The calibration interval needed so that the reconstructed input signals remain within the target uncertainty band has also been studied.

II. DESCRIPTION OF THE SAMPLING SYSTEM

The block diagram of the $\Sigma\text{-}\Delta$ sampling system is shown in Fig. 1. In addition to the system reported in [2], two improvements have been made. Firstly, the immunity of the voltage reference circuit to digital noise from the rest of the board was improved. The ADC chosen for this work [3] demands a differential signal between 0 V and its reference voltage. In this second revision, the fully differential amplifier (FDA in Fig.1) derives the corresponding voltage from an additional output of the voltage reference.

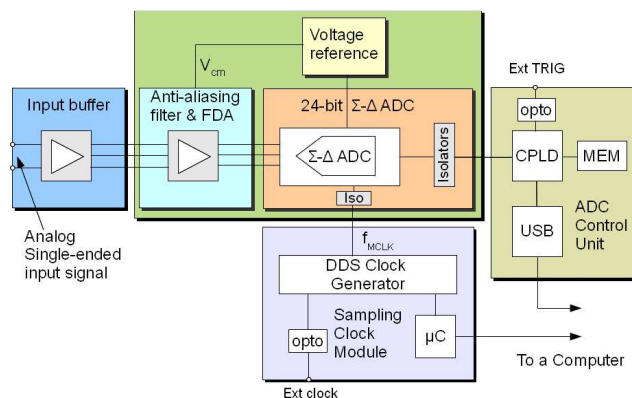


Fig. 1. Block diagram of the $\Sigma\text{-}\Delta$ sampling system.

III. MODEL OF THE SYSTEM

A. The System Model

Fig. 2 depicts a simplified block model for the complete sampling system, where the transition from the analog into the digital domain is indicated by the dotted line. The analog part

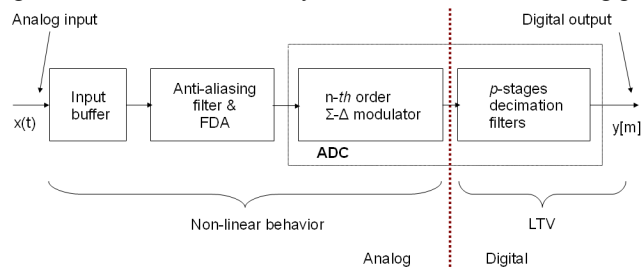


Fig. 2. Model of the sampling system.

consists of the input buffer, the fully differential amplifier and the n -th order modulator of the $\Sigma\text{-}\Delta$ ADC. The digital part includes the p -stages decimation filters. All non-linear behavior has been grouped in the analog part. As a result, the digital part can be described using a linear time-varying system LTV [4]. The Hammerstein model [5] can be used for systems with these characteristics, as it consists of a non-linear block followed by a linear block. In this work, the non-linear block is parameterized in terms of a fourth order polynomial, while the linear block models the overall frequency response of the digital FIR filters inside the ADC chip.

B. The Model for Post-Compensation

When an input signal is acquired, no “a priori” information about its characteristics should be assumed. The only

information available is the time series of numerical values at the output of the sampling system, $y[m]$. In order to reconstruct the input signal, $x(t)$, the inverse transfer function of sampling system needs to be applied to $y[m]$. This can be carried out using the Wiener block model, which consists of a linear block at its input followed by a non-linear block [5]. The linear block corrects the deviations in $y[m]$ due to the non-ideal gain of the digital FIR filters in the ADC. The non-linear block is the inverse fourth order polynomial of the analog part in the Hammerstein model and reconstructs a sampled version of the continuous time signal $x(t)$.

IV. IDENTIFICATION OF PARAMETERS IN THE SYSTEM MODEL

Two sets of parameters can be identified separately. A JWS [6] was programmed to generate triangular waveforms with 16 steps per period at different frequencies and amplitudes. A least-squares fit to a fourth order polynomial was then performed between the Josephson values and the ADC readings. For the LTV block, the gain deviation at dc, established with the waveforms from the JWS, was used to correct the inverse transfer function.

The stability of the model parameters was also evaluated. In the short term, the Josephson calibration was repeated daily over one week. A medium term evaluation was performed after two additional months, with the system left powered continuously. The drift of the transfer function for both intervals is considerably lower than $6 \mu\text{V/V}$ [1]. At the level of uncertainty targeted in this work, Josephson calibrations would be required less frequently than every three months.

V. VALIDATION OF THE SYSTEM MODEL

In order to establish the quality of the approach adopted in this work, a validation procedure was performed through a comparison with a high accuracy digital voltmeter (DVM), the Agilent model 3458A¹. An ac calibrator generated sinusoidal

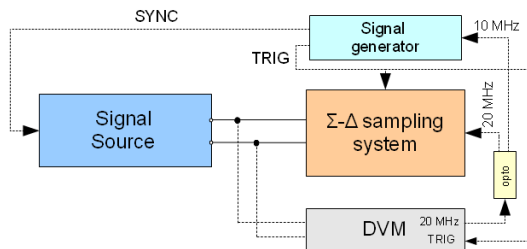


Fig. 3. Measurement setup for validation.

signals in the frequency range between 62.5 Hz and 2 kHz with amplitudes of 1 V. The two sampling systems were connected as illustrated in Fig. 3. The sampling parameters for the DVM were chosen to provide its best uncertainty at each signal frequency. The results for 500 Hz are depicted in Fig. 4

¹ Identification of commercial equipment does not imply endorsement by PTB and INTI stating that the equipment is the best available for the purpose.

and show excellent agreement between the two systems. Furthermore, the uncertainties show that the Σ - Δ sampling system provides a lower uncertainty than the DVM for sampling rates below 32 kHz.

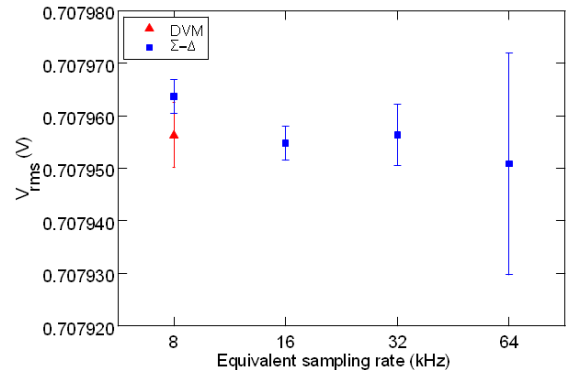


Fig. 4. Results of the model validation at an input signal frequency of 500 Hz. The uncertainty bars correspond to $k=1$

VI. CONCLUSIONS

A sampling system based on a Σ - Δ ADC has been built and characterized. Its transfer function has been modeled and the parameters of the model measured using Josephson waveforms. The model has then been used to reconstruct the signal at the input terminals from the readings of the ADC. The experimental results confirmed that the estimated combined relative uncertainty is $8 \mu\text{V/V}$ ($k=1$) at equivalent sampling rates lower than 32 kHz.

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