Arbitrary function generator using Direct Digital Synthesis

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***Abstract* — This paper describes the development of an arbitrary function generator based on Direct Digital Synthesis (DDS) technique. This signal generator is capable of generating single-tone sinusoidal (THD < -80 dBc), two-tone sinusoidal, square wave, triangular and sawtooth waveforms in the frequency range from 0 to 10 kHz. The frequency stability achieved is 3.9 μHz (τ = 2 s) and the amplitude stability is 2.0 μV (τ = 2 s).**

***Index Terms* — Measurement, frequency measurement, amplitude modulation, signal generators, distortion.**

I. Introduction

This work extends the facilities and performance analysis of the system described in [1]. This new system can be used not only for ADC characterization as indicated in [1] but also in other areas, such as time and frequency measurements, calibration of sound level meters and calibration of electrocardiograph.

In comparison with phase locked loop (PLL), this method allows to synthesize precise frequencies using low-cost commercial devices (e.g. with a 48-bit DDS a frequency resolution of 1.421 nHz can be achieved). Furthermore, this technique has a low transient time to the output frequency and few space requirements (commercial devices have small packaging).

II. Theory of Operation of Direct Digital Synthesis

DDS technology consists in using digital signal processing to generate signals at different frequencies selectable by software from a reference clock.

A simplified block diagram of a DDS is shown in Fig. 1. The block diagram consists of four blocks: a reference clock, a phase accumulator, a look-up table and a digital-to-analog (D/A) converter. The theory of operation can be summarized as follow: the phase accumulator sums at each clock pulse the tuning word. Thus, its output is a digital ramp (binary code). The look-up table converts the phase accumulator output in a digital sine. Finally, the D/A converter transforms the digital sine into an analog signal.

The relationship between the tuning word, the clock reference, the number of bits of the DDS and the frequency of the output signal is shown in (1), as proposed in [2],

$$f_o = M \frac{f_{clock}}{2^N}, \quad (1)$$

where f_o is the output frequency, M is the tuning word, f_{clock} is the reference clock frequency and N is the phase accumulator resolution.

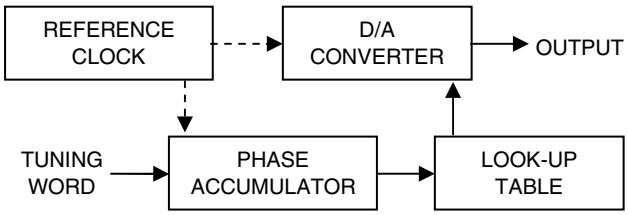

Fig. 1. Simplified block diagram of a DDS

III. System Description

Figure 2 shows a simplified block diagram of the developed system. The reference clock can be either internal or external set by a clock selector, which is controlled by a microcontroller. The clock provider block delivers the clock signal to the system and to an output for synchronization with other systems.

The generation of a two-tone sinusoidal signal was done combining the output of two AD9852 (A and B in Fig. 2). Single-tone sinusoidal was obtained by the AD9852-A. Because the AD9852 is only capable to synthesize sine and square waveforms, a third DDS (AD9834) was used to generate triangular and sawtooth waveforms.

Phase accumulator truncation [3] and the DDS internal D/A converter [4] contribute to the total harmonic distortion (THD). To minimize their effects, the output signal of the AD9852 was filtered by a third order Butterworth lowpass passive filter. To reduce the system noise the filters were made with passive components, as suggested in [5]. Besides, the Butterworth topology was used because of the flatness characteristic in the passband, hence the signal amplitude is attenuated by the same gain deviation in the frequency band of interest.

The amplitude of the output signal of the DDS device is limited to 1 V. To amplify the signals and not to degrade the THD of the system, low distortions programmable gain amplifiers (PGA) AD8250 were employed to remove spurious frequencies generated by the PGAs, their output were also filtered by the same filter topologies as in the case of the DDS devices.

Finally, to combine the outputs of the AD9852-A and AD9852-B to generate the two-tone signal, an adder and a multiplier circuits have been designed.

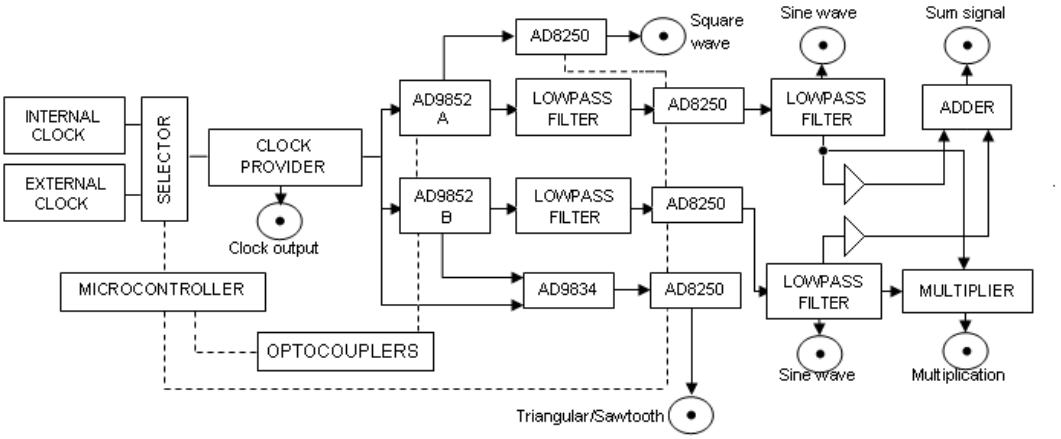

Fig. 2. Simplified block diagram of the complete system

The hardware was mounted in a two-layer PCB which was toughly designed in order to avoid interference between tracks.

Some modifications were done to the system presented in [1]. One of them was the inclusion of optocouplers to minimize noise between the microcontroller and the AD9852. Other important modification in order to avoid crosstalk between channels was to buffer the filtered output of the AD8250.

IV. Results

A. Frequency and Amplitude Stability

To determine the frequency and amplitude stability the system was programmed to generate a sinusoidal waveform with nominal frequency of 62.5 Hz and nominal rms amplitude of 0.23 V. The stability was obtained computing the Allan variance on the measured data. The results are shown in table 1 for an observation time $\tau = 2$ s.

Table 1. Frequency and amplitude stability ($\tau = 2$ s) of the arbitrary function generator output.

Output frequency	Frequency stability	Output amplitude	amplitude stability
62.539086 Hz	3.9 μHz	0.227902 V	2.0 μV

DDS technique is based on digital signal processing, thus it does not introduce instability to the output frequency. As a consequence, the contribution to the instability in frequency depends on the reference clock.

B. Total Harmonic Distortion

The measured and simulated THD results listed in table 2 show that the designed system can achieve a THD of -80 dBc.

Table 2. Total harmonic distortion of the system.

Measured	Simulated
-80.37 dBc	-80.62 dBc

V. Conclusion

The designed arbitrary function generator can achieve a THD < -80 dBc, a frequency stability of 3.9 μHz and an amplitude stability of 2.0 μV when generating single-tone sinusoidal. This device can be used in measurement schemes which require alternating signals as source.

Measurements of the total system performance will be included at the full paper.

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References

[1] W. Adad and R. Iuzzolino, “Low distortion signal generator based on direct digital synthesis for ADC characterization”, SEMETRO IX Conf. Digest, September 2011.

[2] Analog Devices, Inc. “A technical tutorial on Digital SignalSynthesis”, 1999.

[3] A. Torosyan and A. Willson, “Analysis of the output spectrum for direct digital synthesizers in the presence of phase truncation and finite arithmetic precision”, 2001.

[4] D. Buchanan, "AN-237: Choosing DACs for Direct Digital Synthesis", Analog Devices, Inc.

[5] K. Lacanette, “A basic introduction to filters – active, passive and switched capacitor NI”, *Application Note AN-779*, 1991.