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Electronic transport in sub-micron square area organic field-effect transistors

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Scaling down organic field effect transistors to channel areas well below the micron square could improve positively its speed and integration capabilities. Here, we report a careful study of the electronic carrier transport for such nanoscale devices. In particular, we explore the validity of standard analysis for parameters extraction in this size regime. We also study the effect of the large longitudinal electric field and fringe currents, especially their influence on the ON/OFF ratio. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4795014]

Organic semiconductors can be integrated as active channels in field-effect transistors (FETs), mostly with the objective of producing low-cost or flexible electronic applications.[1–8] In the scientific literature, organic FETs (OFETs) are devices whose channel lengths typically range from the millimeter down to the micrometer level and very commonly have interdigitated electrodes. These geometries are necessary for producing a large, easily measurable, output current since organic semiconductors have very low carrier density. Operative frequencies for these OFETs are also limited to the kHz regime,[9,10] due to the relatively low carrier mobility of the semiconductor channels (rarely much in excess of $1\,cm^2/Vs$ (Refs. 3, 6, and 11)). In this scenario, miniaturization and improvement of OFETs well down into the sub-micrometer regime are very much sough-after technological improvement. Recent reports using organic circuits show that even a relatively modest improvement in size and speed would be highly desirable for practical applications.[12,13] Shortening the channel length in OFETs leads to an increase in switching speed, since this parameter is roughly inversely proportional to the square of the channel length.[9] Moreover, smaller devices with active areas below $100\,nm^2$ could be integrated at a higher density, increasing the overall functionality of a circuit per unit area. From another perspective, sub-$100\,nm^2$ devices are going to be most likely constituted by one single crystalline grain of the organic material, so the undesirable role of defects and grain boundaries on the electronic carrier transport will be removed or at least greatly decreased.[14–16]

However, all these possible advantages are countered by several problems. In nanometer-sized OFETs, transport is commonly dominated by the contact resistance rather than by the bulk of the organic material.[17–19] In addition, reducing the organic semiconductor area in an OFET generally leads to a significant increase of the strength of the longitudinal electric field along the channel and to significant fringe currents.[20–23] In this operational condition, the standard formulas for studying carrier transport in OFETs do not longer apply and consequently, the parameters extracted from them are dubious.

In this letter, we present pentacene-based OFETs with channel areas much below the μm^2 in which spurious effects in the carrier transport cannot be neglected. In this context, we propose a method for calculating a corrective form-factor for the standard expressions generally applied to transport in OFETs. The use of such corrective factor allows us to extract relevant physical parameters that are not correct without this adjustment, such as the field effect mobility, the intrinsic conductivity of the channel, and the ON/OFF ratio.

For our experiments, we fabricated bottom-gate, bottom-contact OFETs with the geometry presented in Fig. 1(a). Channel lengths (L) from 320 nm down to 120 nm were used in this study. The metal contacts (palladium: 20 nm thick) were defined by e-beam lithography (EBL) and lift-off on highly doped p-type Si substrates that act as a common gate. Channel widths were kept constant for the drain (W1: 100 nm) and source (W2: 500 nm). Different widths of the electrodes were used for making our transistors geometry as general as possible. The gate dielectric is a 150-nm-thick thermally grown SiO_2 layer. Pentacene was deposited by organic-molecular beam deposition (OMBD) in UHV conditions (base pressure $<1\times10^{-9}$ mbar; evaporation pressure $<1\times10^{-8}$ mbar). Pentacene thickness was 58 nm, deposited (through a shadow mask) at a rate of 1 nm/min on substrates kept at room temperature and without primer. It is widely accepted that, in general, both using a primer for the gate dielectric, and functionalizing the channel electrodes largely improve the response of organic transistors.[17] Nevertheless, here we choose to keep our devices as simple as possible for studying the effect of the channel area reduction. Fig. 1(b) shows a scanning electron microscopy (SEM) image of one of the devices. The electrical measurements were performed in a LakeShore probe station under vacuum (10^{-5} mbar) and in the dark. We used two Source-Measure Units (SMUs) of a Keithley 4200 Semiconductor Characterization System with sub-femto preamplifiers for supplying the gate voltage (V_{GS}) and the channel bias voltage (V_{DS}). Both the gate current (I_{GS}) and the drain current (I_{DS}) were measured, but only the

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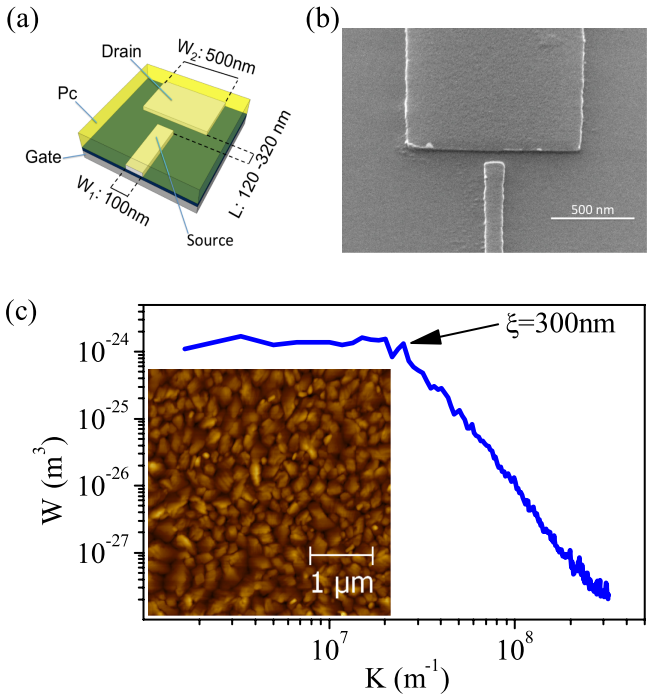

FIG. 1. (a) Scheme of the nanometric OFET showing the nominal dimensions as defined by electron-beam lithography. This specific geometry is characterized by three parameters: the channel length (L) and the width of the source (W_1) and drain (W_2) electrodes. (b) SEM image of fabricated metallic electrodes, showing a nanogap. (c) PSD of an AFM image of a pentacene film. From the PSD, the typical grain size can be inferred. The inset shows the AFM image of pentacene.

latter is reported here. The gate current was constantly monitored to ensure that there was no significant leak through the gate. The organic semiconductor morphology was checked by means of atomic force microscopy (AFM, inset in Fig. 1(c)). The pentacene films present pyramidal grains with a characteristic size of 300 nm, as derived from the power spectral density analysis (PSD) (Fig. 1(c)).[24]

In Fig. 2(a), we show the representation of I_{DS} as a function of V_{DS} for a transistor with a channel length of 260 nm. Curves for other channel lengths are analogous and are not shown. Nanoscale devices typically show current-voltage curves with a linear behaviour at low source-drain bias, a clear saturation at large source-drain voltages and very good modulation for different gate voltages. These curves compare favourably with those of transistors with micrometre length channels widely available in the literature (see Refs. 6, 11, and references therein).

The modulation of the current in the semiconducting channel is clear in the transfer characteristics, in which we plot I_{DS} versus V_{GS} (see Fig. 2(c) for transistors with different channel lengths). As expected,[25] the ON/OFF ratio is reduced with decreasing channel length, moving from more than four orders of magnitude for a 320 nm channel to less than one for transistors with 120 nm channels. Similar transistors with micrometric channel have ON/OFF ratios of six orders of magnitude.[26] It is also evident from the transfer characteristics that the nanosized transistors do not switch off completely, having a relatively large $I_{DS,OFF}$ current (Fig. 2(b)). This is a usual feature for devices similar to those reported here (see Ref. 25 and references therein). Transfer characteristics are particularly useful for the extraction of the field-effect mobility.[21,27]

For the sake of clarity, we must specify the criteria followed in all the discussion. We consider the transistors to be in OFF state when the positive gate bias stops modulating the drain current; above L = 300 nm, the OFF current was found to be below the sensitivity of the instrument. The ON state is considered in the linear regime ($|V_{GS}\text{-}V_T| < |V_{DS}|$), where V_T is the threshold voltage or voltage below which the transistor is in OFF state. In both cases, we are at the limit of the region for which the gradual channel approximation holds and the devices present little or no short channel effects, i.e., the transverse electric field generated by the gate bias is larger than the longitudinal electric field generated by the channel bias, and hereafter simply referred to as E.[28,29]

We first analyze the transistors in the OFF state. Representative curves showing a linear relationship between $I_{DS,OFF}$ (extracted from the transfer characteristics) and V_{DS} for different channel lengths are presented in Fig. 2(b). For the geometries used here, the total current flowing through the channel is larger than the values which would be expected by considering the infinite-parallel-plate approximation. In the literature, these extra currents are commonly referred to as fringe currents.[22,30] A form-factor that accounts for this difference in current can be numerically computed for our specific

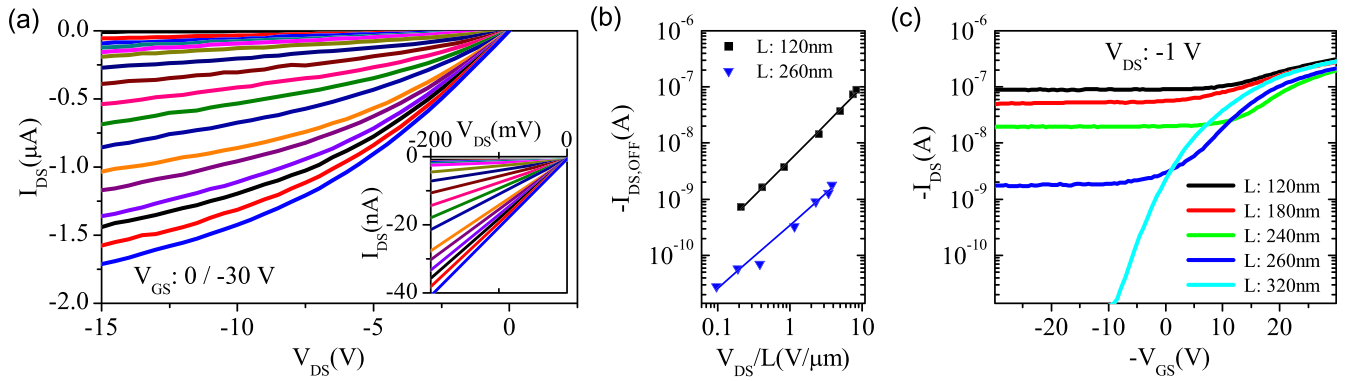

FIG. 2. (a) Source-drain current (I_{DS}) as a function of source-drain voltage bias (V_{DS}) represented for different gate-source (V_{GS}) voltages. The main panel shows the clear tendency to saturation of the current-voltage curves for relatively low voltage bias of around 15 V. The inset is a magnification of the main panel for small source-drain voltages ($V_{DS} < 0.2$ V). In this inset, the linear regime in the source-drain current is more evident. (b) Source-drain leakage current ($I_{DS,OFF}$) as a function of the channel bias normalized by L. (c) Transfer curves or representation of the source-drain current (I_{DS}) as a function of gate-source (V_{GS}) for different channel lengths.

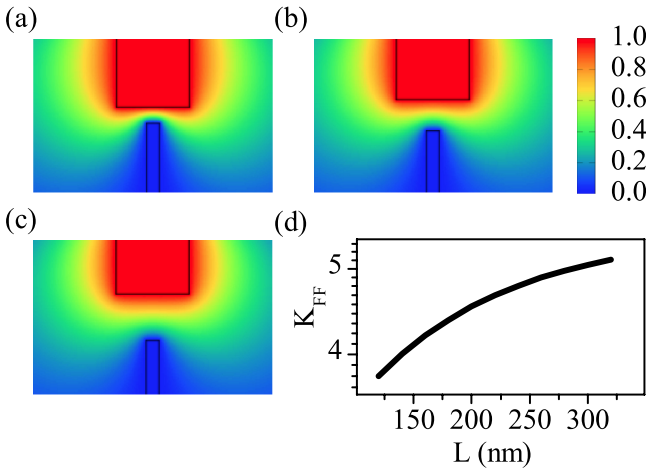

FIG. 3. (a)-(c) Color-code representation of the electrostatic potential between the source and drain electrodes, as calculated from the Laplace equation. In the figure, which represents different channel lengths, it is clear how the small channel length to channel width ratio distorts the electrostatic potential distribution. The fringe current is, therefore, affected in a similar fashion following the electrostatic potential. (d) Form factor K_{FF} as a function of the transistor channel length. The specific values represented in the figure arise from the exact calculation of the current in the transistor geometry used in this manuscript and cannot be readily extrapolated to other geometries.

transistor geometry. This form factor k_{FF} is the ratio between the conductance G of a conductor with the shape proposed in Fig. 1(a) and the ideal conductance calculated in the parallel-plate-approximation with distance between the electrodes L and width W_1 (see supplemental material)[37]

$$k_{FF}(L) = \frac{G_{\text{proposed shape}}(L, W_1, W_2 = 5W_1)}{G_{\text{infinite-parallel-plate approximation}}(L, W_1)}. \quad (1)$$

Fig. 3 shows the computed potential distributions in the channel and the values obtained for k_{FF} as a function of the channel lengths. Then, we express the linear behavior of $I_{DS,OFF}$ in terms of a ohmic conductivity of the channel when the device is in the OFF state, σ_{OFF}, by correcting the standard formula for the conductivity of a homogeneous media by k_{FF} as

$$I_{DS,OFF} = k_{FF} \cdot V_{DS} \cdot \sigma_{OFF} \cdot \frac{W_1 \cdot t}{L}; \; L < 300\,\text{nm}, \quad (2)$$

where t is the effective thickness of the semiconductor layer. Note that our calculation of the electrostatic potential, as the experimental results shown above, is as general as possible since we consider two metallic electrodes with different widths, W_1 and $W_2 = 5\ W_1$. In the case of a more conventional geometry with $W_1 = W_2 = 100\,\text{nm}$ and $L = 220\,\text{nm}$, the calculation method leads to a k_{FF} value of 3.43. In the extreme case in which W/L tends to infinite, the fringe current contribution is negligible and k_{FF} tends to 1.

Following the characterization of the transistors in the OFF state, we can proceed with the study of the device in the ON state. The standard expression for long-channel crystalline OFETs in the linear regime has to be modified considering three different assumptions:[28,31,32] first, it has to account for the lack of validity of the infinite-parallel-plate approximation previously mentioned; second, the field-effect mobility should be corrected by the longitudinal electric field;[20,21] third, the introduction of I_{OFF} as an offset. We then propose the following equation:

$$I_{DS} \approx k_{FF} \frac{W_1}{L} \mu C_i (V_{GS} - V_T) V_{DS} + I_{DS,OFF};\; V_{GS} - V_T > V_{DS}, \quad (3)$$

where V_T is the threshold voltage and C_i the dielectric capacitance of the gate per unit area. The mobility $\mu = \mu^0_{FET} \exp(\beta' \sqrt{V_{DS}/L})$ accounts for the Frenkel-Poole dependence on the longitudinal channel electric field, being β' the temperature-corrected field-dependent coefficient and μ^0_{FET} the zero field mobility.

The introduction of k_{FF} must be supported by a linear dependence of I_{DS} vs. V_{DS}. This is experimentally observed in the low V_{DS} region of the output characteristics presented in the inset of Fig. 2(a). Also, a set of mathematical considerations support this procedure.[33,34] Besides, the carrier density in the accumulation layer (formed by the gate bias in the ON state) decays in the regions of the pentacene film relatively far (in terms of L) from the most active part of the channel. This would confine the extension of the fringe currents. The longer current paths, therefore with lower net contribution, would be modified with respect to the OFF state and require higher order corrections in the k_{FF}. In this work, we neglect this effect. Note that k_{FF} is a function of L and $I_{DS,OFF}$ is a function of V_{DS}, even if here we are not making it explicit.

Once we have the expression for the I_{DS}, we can differentiate it in V_{GS} and operate accordingly to obtain

$$\frac{L}{W_1 C_i V_{DS}} \frac{dI_{DS}}{dV_{GS}} \approx k_{FF} \mu^0_{FET} \exp\left(\beta' \sqrt{\frac{V_{DS}}{L}}\right), \quad (4)$$

where the left-hand side resembles the standard procedure for extracting the field-effect mobility from the linear region of the transfer characteristics.[21,27] In order to obtain

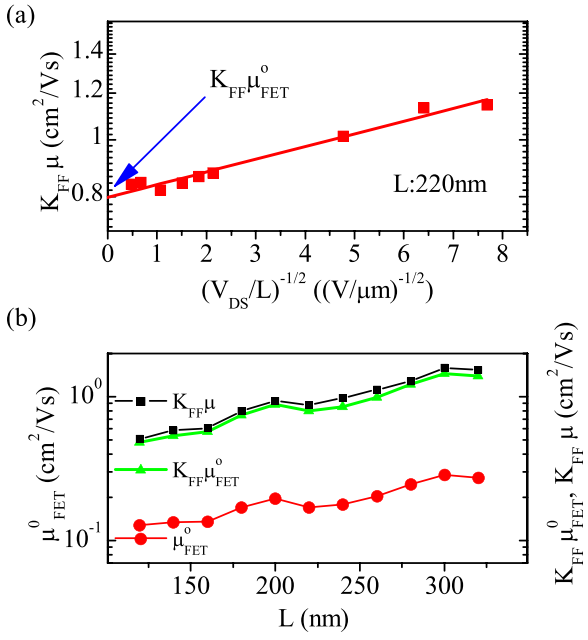

FIG. 4. Procedure to extract the zero field mobility. (a) Slope of the transfer characteristic ($\mu k_{FF} = dI_{DS}/dV_{GS}(W_1 C_i V_{DS})^{-1} L$ in log scale) as a function of the applied voltage to the semiconducting channel. The extrapolation of the curve allows the extraction of the uncorrected zero-field mobility ($k_{FF}\mu^0_{FET}$). (b) Zero-field mobility (μ^0_{FET}) as a function of the organic transistor channel length. For comparison, also $k_{FF}\mu^0_{FET}$ and $k_{FF}\mu$ are plotted.

the zero-bias field-effect mobility, we proceed in three steps; first, we extract the slope from the linear region of the transfer characteristics at several bias voltages; second, $\mu^0_{FET} \cdot k_{FF}$ is obtained from the linear regression in the plot $\ln[dI_{DS}/dV_{GS}(W_1 C_i V_{DS})^{-1} L] = f(\sqrt{V_{DS}/L})$ (Fig. 4(a)); and third, each value is normalized by the proper value of k_{FF} for each specific L (Fig. 4(b)).

This procedure allows us to extract the real values of the zero-field mobility, dealing with the fringe current contribution that is generally overlooked when extracting organic semiconductor mobility values (see, for example, the values listed in Ref. 25). For the sake of comparison, in Fig. 4(b), we represent the corrected zero-field mobility values together with those values that would be obtained without taking into account the size and shape of the metal electrodes via the form-factor k_{FF}. With the proposed procedure, the mobility values found (around 0.2 cm^2/Vs) are consistent with the literature reports for the materials and fabrication techniques used here. Even if the overall correction does not exceed one order of magnitude, in our specific case, the uncorrected values are in excess of 1 cm^2/Vs and unrealistic for the materials and fabrication methods reported here.[11,24,35,36] Mobilities of the order of 0.01 cm^2/Vs were measured in transistors with interdigitated geometries and channel lengths of 2 μm, fabricated simultaneously on the same substrate and following the same procedures.[21] For our nanometer-sized transistors, the dependence of the zero-field mobility with L may be affected by two factors; the detrimental effect of having an L comparable to (or smaller than) the extension of the contact region,[17] and the beneficial effect of a channel with few grain boundaries. We hypotheses that the scaling between these two factors results in the slowly increasing zero-field mobility we experimentally measure below 300 nm. For micrometer-sized channels, the grain boundaries contribution is predominant.

Combining Eqs. (2) and (3), we can derive an expression that describes the switching capabilities of our devices below L = 300 nm, in the range for which our devices present a strong decrease of the ON/OFF ratio (see Fig. 2(b))

$$\frac{I_{ON}}{I_{OFF}} \approx 1 + \frac{\mu^0_{FET}}{\sigma_{OFF}} \exp\left(\beta' \sqrt{\frac{V_{DS}}{L}}\right) \frac{C_i}{t} (V_{GS} - V_T). \quad (5)$$

Equation (5) emphasizes the detrimental effect of the OFF intrinsic conductivity of the organic film, while highlighting the possibility of improving the ON/OFF ratio by reducing the organic film effective thickness or by increasing the dielectric capacitance of the gate. Beside these well-known conclusions, we remark two further points which go beyond the standard treatment applied to OFETs. First, the form-factor k_{FF} is not present in Eq. (5) indicating that the fringe currents do not play a relevant role in the ON/OFF ratio. This conclusion is actually true only when the device is in the linear regime, since otherwise a corrective factor different from k_{FF} has to be introduced in Eq. (3) that will not compensate the k_{FF} in the $I_{DS,OFF}$. Second, due to the Frenkel-Poole-like dependence of the mobility, increasing V_{DS} (moderately) improves the ON/OFF ratio. This conclusion has a limited practical use since V_{DS} cannot be increased beyond the linear regime, but puts in solid ground the influence of the activation of the mobility at high longitudinal electric fields.

In conclusion, we have reported pentacene field-effect transistors with channel lengths in the order of 100 nm and channel areas much below the μm^2. The devices presented show current-voltage curves with a linear behaviour at low source-drain bias, a clear saturation at large source-drain voltages and very good modulation for different gate voltages. Transfer characteristics, in which the source-drain current is represented as a function of the gate voltage, are typically used for extracting the carrier mobility in the semiconducting channel. Here, we show how the equations commonly employed need to be treated carefully since the total current flowing in a transistor is affected by potentially large fringe currents if the channel width to channel length ratio (W/L) approaches 1. We have computed the influence of the fringe current in the mobility via a form-factor, which depends on the specific geometry of the transistor channel. Finally, we propose a general expression for the ON/OFF ratio in this kind of devices.

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[36]Mobility values for transistors in different chips but with the same geometry show an typical dispersion around 20%, much lower than the correction to the mobility arising from the form-factor k_{FF}.
[37]See supplementary material at http://dx.doi.org/10.1063/1.4795014 for the numerical procedures to calculate k_{FF}.