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Abstract. Precision measurement of DC and AC voltages requires an analogue to digital converter specification to have two key parameter values: the number of effective or noise free bits and the signal bandwidth. Commercial ADCs may offer the potential for use in a metrology class voltmeter but there is no easy way to compare the dynamic specification of a DMM with that of an ADC, especially when the number of bits or bandwidth changes. An architecture independent ADC/DMM figure of merit (FOM), is proposed to facilitate this comparison. At National Measurement Institutes, it is necessary to be able to measure with significantly greater precision than the device or instrument under test. Analysis shows that the FOM required of a metrology class ADC is beyond the state of the art for both ADCs and instruments. Fortunately, the use of superconducting Josephson junction based circuits offers the possibility to achieve the required precision. This paper gives the background to and reviews the progress of an EU funded research project for a quantum analogue to digital converter which is aiming to achieve the required FOM, beyond the state of the art.

1. Background

Ideally, for maximum sampling rate, an analogue to digital converter (ADC) should be a monolithic integrated circuit as this minimises interconnect delays and facilitates maximising the sampling rate. Quantising error is related to the minimum number of bits of resolution required to represent a full scale quantised signal. Thermal noise, sampling jitter, aperture error and circuit non-linearity result in a reduction in the minimum number of bits. Broadly this reduced number of bits is referred to as the effective number of bits (ENOB). Ultimately, the ADC architecture, technology and physics involved in the ADC circuit limits maximum sampling rate, noise and linearity. The optimum selection of these depends on the target application and can be a challenging task as some choices may require beyond the state of the art technology. In order to simplify this task, several figure of merit (FOM) equations have been proposed for ADC performance comparisons and surveys based on these have been published [1], [2]. The one used later in this present paper is based on the aperture error and effective number of bits

and has been used for some time [3]. This FOM is simply the effective number of bits added to $\log_2$ of the bandwidth.

2. Progression of state of the art

Considering only the physics aspects, the use of Josephson junction based superconducting circuits could minimise thermal noise and maximise sampling rate and therefore increase FOM. It is possible to make an entire ADC from superconducting components, however, the number and type of components on a superconductor IC is very limited and this has led to the choice of one ADC architecture, the one bit sigma delta ADC [4]. This employs inductor based loop filters, a Josephson junction (JJ) comparator, and a JJ one bit DAC. Practical ADCs have been reported [5] but have indicated that the lowest signal frequency or narrowest bandwidth practical is limited by the size of the inductor. The stability of a modulator of higher than second order depends on the precision of component values which determine loop gain. In practice this means that only first and second order DSMs have been reported. Typically the minimum bandwidth is 10 MHz [6]. Loop update rates of 100 GHz have been reported but as the loop order is limited, a high oversampling factor (ratio of half sampling frequency to signal bandwidth) is required to achieve a useful ENOB. A survey has shown that these superconducting RF type ADCs have a similar figure of merit to state of the art semiconductor ADCs [6] so the application is aimed at other potential aspects of a superconducting ADC such as perfect linearity. However, linearity has proven difficult to confirm as tests are limited by the noise and non-linearity of RF analogue signal sources [4]. An alternative ADC design is to use arrays of Josephson junctions, fabricated with high reproducibility (see for example [7]) combined with room temperature electronics.

3. Josephson Junction aspects

So far we have considered only the dynamic aspects of the ADC specification. From a metrology point of view a unique advantage of a JJ based ADC is that its reference voltage is defined by the values of fundamental constants in quantum physics so has precision and stability well beyond any other ADC technology. As all JJ quantising steps are the same value, this promises perfect linearity from a programmable JJ chip. There are two approaches to the generation of quantum accurate voltage waveforms; programmable and pulse driven Josephson junction systems. For reviews of the two technologies see [8],[9]. In programmable systems a binary segmented Josephson junction array of 10,000 or more junctions in series is used essentially as a digital to analogue converter. In the pulse driven system the Josephson junction array is employed in a Sigma Delta D to A converter. Please note that for historical reasons, in the literature, Sigma Delta (SDM) and Delta Sigma are used interchangeably and refer to the same topology

A key application area of this JJ based metrology is to provide quantum traceable voltage standards for National Measurement Institutes. A chip which has a large number of JJ in series has enabled DC calibration and arbitrary waveform generation (AWG) with performance exceeding that of conventional instruments. National Measurement Institutes have performed experiments to characterise the best available commercial AC/DC voltmeters [10]. Most characterisation measurements have been aimed at DC to 20 kHz as this is where most high resolution and high precision instruments and ADCs are focussed. This application area is one this paper will now consider in more depth.

4. Limits to dynamic Measurement of JJ based ADC and DAC

The question that remains is, how can we be sure that dynamic measurement figures of the linearity of a JJ AWG [11], such as spurious free dynamic range, are not in reality better than can be measured by commercial instrumentation. What we need is a JJ based ADC covering the range DC to 1 MHz. The

introduction to this paper indicated that examples of JJ based ADCs are available only for RF applications. Research in Europe [11] has produced a first order one bit SDM ADC experimental system with a JJ DAC and signal bandwidth DC to 20 kHz. The system consists of interconnected commercially available modules external to the cryostat which contains only the JJ DAC. System ENOB was not expected to be state of the art as it was a first order one bit SDM with an oversampling factor of 1000. This was chosen to avoid stability and delay issues. In comparison, semiconductor SDM ADCs are fourth or higher order loops so have higher ENOB. At this point we will consider the FOM of some state of the art 32 bit ADCs (a) ADI AD7177-2, (b) TI ADS126X32B, (c) LTC LTC2508-3, which have potential applications in the DC and AC voltmeter area and compare this with the FOM of a state of the art DC/AC voltmeter (HP 3458A). From the manufacturers data sheets, a comparison with a 1 kHz sinewave signal was selected. Unsurprisingly it was difficult to extract the information as 'noise free bits' and ENOB were taken to be the same value. The best data sheet specification appeared to be 20.2 ENOB and this gives a 1 kHz FOM of 30.2. The HP3458A has been tested against a quantum accurate voltage source [12] at National Measurement Institutes worldwide and published information [13] indicates an equivalent ENOB of 22 for a 1 kHz sinewave. Its FOM is therefore 32 . For any quantum accurate ADC to be able to confirm the purity of the test signal, its quantising error must add less than the quantising error of the waveform. The actual specification depends on the tolerance specified. For example, if the added error is less than 0.1 dB then a 24 bit linear sine wave may be required to test the 22 bit ADC. Hence in order to test the 24 bit sine wave to the same uncertainty we would need a 26 bit linear ADC able to digitise 1 kHz. Clearly this is beyond the state of the art but could be required by standards laboratories. Even more challenging would be to extend this specification to 1 MHz signals. The Euramet funded EMPIR project "QuADC" which is part of the EU Horizon2020 scheme seeks to meet this challenge.

5. QuADC

The aim of the QuADC project is to design and build a quantum voltage digitizer based on pulse driven Josephson junction arrays. The system will include room temperature Sigma-Delta electronics, a pulse generation system and a feedback loop. The system will be capable of quantum accurate characterisation of arbitrary voltage waveforms. The quantum voltage digitizer will operate over DC to 1 MHz frequency range with a target uncertainty of 10 nV/V for frequencies up to 1 kHz and better than 10 μV/V for frequencies up to 1 MHz . The sampling rate will be 100 MHz or 20 MHz and the input voltage will be ±1 V maximum. The system will be based on Sigma-Delta topology integrated with conventional telecoms optoelectronics and commercial FPGA (field programmable gate arrays) for data processing. The main technical challenge will be to optimize the system for such a broad input frequency range. Careful design, simulation and testing will be required to reach the challenging uncertainties given above.

The required dynamic uncertainty specification for this system in nV/V was translated into ENOB and this resulted in 27 at 1 kHz (FOM 37) and 17 at 1 MHz (FOM 37), compared with the 32 FOM of the DMM and 30 of the ADC. It is also interesting to note the constant FOM of 37 indicates that both specifications could be achieved using one ADC architecture, followed by a digital filter which would increase the ENOB by one for each halving of the bandwidth. Maximum oversampling ratio requires minimum loop delay and until the system units are interconnected, estimates have been used for setting minimum and maximum expected oversampling ratios. The architecture chosen was a multibit 4th order continuous time loop with loop update frequencies of 20 to 100 MHz . In order to accommodate this range it was necessary to provide an analogue loop filter design that was reconfigurable on its printed circuit. The present status of the project is that a high order continuous time Sigma Delta modulator has been designed and some aspects have been simulated, constructed and measured. Simulation results

have shown that the attenuation of the in-band quantization noise by the NTF gives an ENOB of 17 bits for high frequency input signals.

6. Conclusions

The background to the QuADC project has been introduced together with an FOM figure that relates DMM specification to ADC performance. Details of the QuADC block diagram and SDM configuration will be presented in a future publication and by the time of the conference it is expected to have built and tested the circuit.

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